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Ph. D. DISSERTATION

Analysis on Characteristics and
Trapping Mechanism of Trap Sites
inside Dielectric or Drain Causing
Random Telegraph Noise in Trap-
Assisted Tunneling GIDL

Trap-assisted 터널링 GIDL 전류에서 RTN을
발생시키는 절연체 또는 실리콘 내부 트랩 사이트
특성과 트래핑 메커니즘 분석

BY

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DEPARTMENT OF ELECTRICAL AND
COMPUTER ENGINEERING
COLLEGE OF ENGINEERING
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지도 교수 신 형 철

이 논문을 공학박사 학위논문으로 제출함
2016 년 2 월

서울대학교 대학원
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ABSTRACT

Variable retention time (VRT) phenomenon is one of the main sources which degrade the retention time of DRAM cell, and this phenomenon becomes recently serious issue in DRAM cell transistor. Through various researches, it is revealed that the origin of VRT phenomenon is gate-induced drain leakage (GIDL) current random telegraph noise (RTN). Thus, comprehensive analyses on traps causing GIDL current RTN should be implemented in order to accurately understand VRT phenomenon. So far, researches on GIDL current RTN in band-to-band tunneling (BTB) current region have been mainly conducted. The characteristics of trap-detrap site causing RTN in BTB GIDL current have been analyzed in various literatures based on the GIDL RTN measurement data. However, with device and supply voltage scaling, researches on GIDL current RTN in TAT region become important topics since GIDL current through trap-assisted tunneling (TAT) mainly flows in the low supply voltage region. And, on the contrast to other current RTN, two trap sites (trap-detrap site and generation-recombination site) cause RTN in TAT GIDL current, which suggests that more characteristics should be accurately analyzed. Nevertheless, there are great lack of the researches on TAT GIDL current RTN and several weaknesses for accurately extracting the characteristics of trap sites.

In this thesis, two trap sites causing GIDL current RTN in TAT current region were physically analyzed. The depth and energy level of traps were extracted based on the measurement data in TAT GIDL current RTN in case of trap-detrap site inside silicon

dioxide. And, the method for extracting the distance between two trap sites was proposed and the distance between two trap sites was actually extracted using the ratio between two TAT GIDL current levels and proper effective permittivity of two different materials.

Second, trapping mechanism was also determined using activation energy comparison of time constants. And, RTN in GIDL current was for the first time measured as a result of electron trapping from conduction band rather than from valence band.

The GIDL current RTN in Buried-Gate CAT (BCAT) array which is used as DRAM cell transistor was actually measured. Especially, the method for extracting the trap characteristics was explained as trap-detrap site was located inside silicon (drain region) as well as conventional trap-detrap sites located in the dielectric or at interface for the first time. The physical characteristics of two trap sites was actually analyzed in case of trap-detrap site inside drain region based on the measurement data of RTN in TAT GIDL current. The researches explained in this thesis provide the insight for understanding and analyzing the GIDL RTN in TAT current region. Moreover, these can be useful in order to understand VRT phenomenon and research the method for reducing VRT phenomenon.

Keywords : Trap-assisted tunneling GIDL current RTN, trap-detrap site, distance between two trap sites, trapping mechanism

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CONTENTS

Abstract	i
Chapter 1. Introduction	1
1.1. Motivation	1
1.2. Scope of thesis	24
Chapter 2. The Extraction of Distance between Two Trap Sites Causing RTN in TAT GIDL Current in case of Oxide Trap- Detrap Site	25
2.1. Introduction	25
2.2. Measurement setup and Background	27
2.3. Accurate extraction of the distance between two trap sites	-- 31
2.4. Results and Discussion	33
2.5. Summary	38
Chapter 3. Analysis on Trapping Mechanism of Trap-Detrap Site Causing GIDL Current RTN	39
3.1. Introduction	39
3.2. Results and Discussion	39
3.3. Summary	48

Chapter 4. Measurement and Analysis on Trap Sites Causing RTN during TAT GIDL in case of Trap-Detrap Site inside Drain Region	----- 49
4.1. Introduction	----- 49
4.2. The depth and energy level of trap-detrap site inside drain region	----- 51
4.3. TAT GIDL current RTN measurement in BCAT cell array	-- 56
4.4. Summary	----- 64
Chapter 5. Conclusion	----- 65
Bibliography	----- 66
Abstract in Korean	----- 71

Chapter 1

Introduction

1.1 Motivation

Thus far, dynamic random access memory (DRAM) cell which consists of 1 access transistor and 1 storage capacitor has been used as main memory cell. The data is stored in the storage capacitor of DRAM cell. The retention time for which the charge state can be retained in storage capacitor without charge loss should be longer than standard refresh time (64 ms) [1]. However, the charge in storage capacitor discharges from the storage capacitor due to the various leakage components in DRAM cell, which results in retention-time degradation [2],[3]. Fig. 1.1 illustrates the various leakage current components in DRAM cell. Among the various leakage current components, gate induced drain leakage (GIDL) current has the largest portion of leakage current components. This means that GIDL current mainly affects the retention characteristics of DRAM cell.

Random telegraph noise (RTN)-like fluctuation in retention time which is called variable retention time (VRT) occurs in DRAM cell, which degrades the retention characteristics of DRAM cell. A part of DRAM cells can become fail bit due to the VRT phenomenon. The VRT phenomenon was reported in many literatures such as Yaney et al. in 1987 [4] and Restle et al. in 1992 [5]. Fig. 1.2 shows the RTN-like VRT phenomenon of DRAM cell reported in above two literatures. Since then, many research groups have

attempted to reveal the origin of VRT phenomenon. In Yuki Mori's literature at 2005, it is reported that the origin of VRT phenomenon is junction leakage current fluctuation as RTN (RTN in GIDL current) [6].

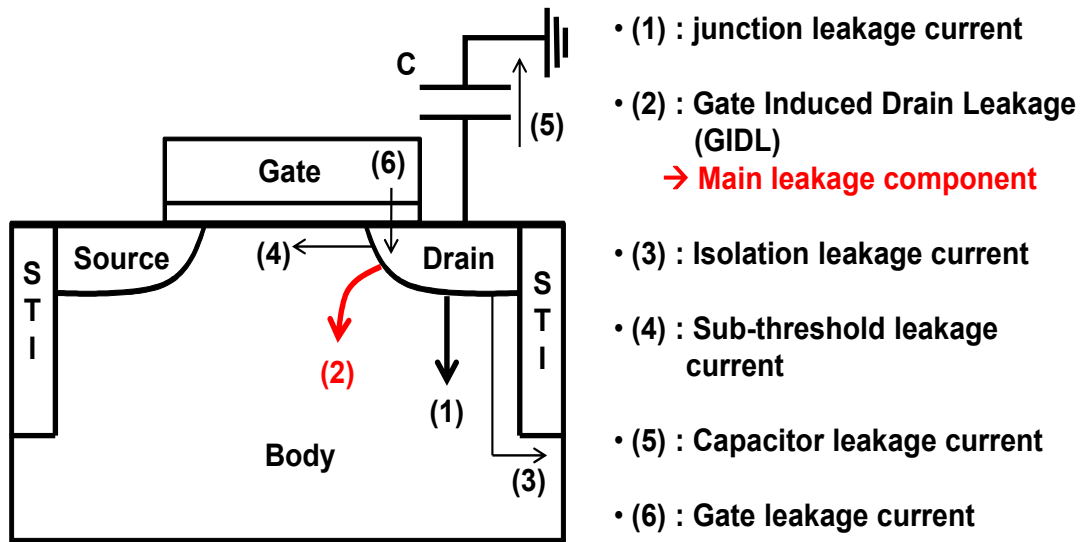


Fig. 1.1 Illustration of leakage current components in DRAM cell

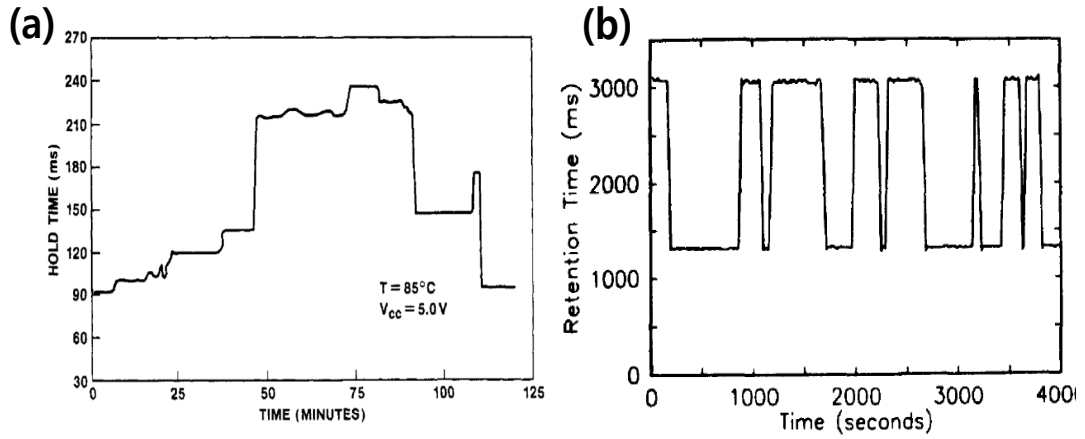


Fig. 1.2 Retention time (hold time) with respect to time : (a) Ref. [4] and (b) Ref. [5]

The RTN in junction leakage current (or RTN in GIDL current) is caused by trap-detrap site. There are various researches on the models of trap-detrap site causing RTN in junction leakage current. In 2006, Ohyu et al. reported that VRT phenomenon was caused by bistable vacancy-oxygen complex defect (V_2O_x) [7],[8]. And, other literatures also reported that RTN in GIDL current occurs by trap-detrap site inside silicon which has bi-stable or multi-level energy states, which can be verified by E_a difference of time constants in GIDL current RTN [6],[9] (structural fluctuation model). Fig. 1.3 shows the lattice configuration of bi-stable trap-detrap site causing RTN in junction leakage current [10].

However, there are other viewpoints for interpreting the RTN in junction leakage current. The viewpoints are that RTN in junction leakage current (GIDL current) is occurred by trap-detrap site in dielectric or at interface. The carrier capture into the trap-detrap site induces electric-field variation at the silicon/dielectric interface, which results

in GIDL current variation [11],[12]. Fig. 1.4 shows the illustration on the electric field variation in energy band diagram with an electron capture into the trap-detrap site. Recently, RTN in GIDL current has been mainly interpreted in the viewppoint of the trap-detrap site in dielectric or at interface.

So far, researches on GIDL current RTN have been almost conducted in band-to-band tunneling (BTB) GIDL current region [11, 13-15]. The physical characteristics (depth, energy level, capture cross section, RTN amplitude) of trap-detrap site causing RTN in BTB GIDL current were extracted in various literatures [11],[15]. First, the equation for the depth and energy level of trap-detrap site was derived using energy band diagram in Fig. 1.5. In order to derive the depth equation of trap-detrap site, grand partition theorem should be used as below equation [13]:

$$\frac{\overline{\tau_c}}{\tau_e} = g \exp\left(\frac{E_T - E_F}{kT}\right) \quad (1.1)$$

In this equation, τ_c and τ_e are capture time and emission time extracted from GIDL current RTN measurement, respectively. The definition of τ_c and τ_e are indicated in below figure (Fig. 1.6). g is the degeneracy factor which is generally assumed to be one, k is Boltzmann's constant, and T is absolute temperature. And, E_T is the energy level of trap-detrap site and E_F is Fermi level of drain region. After expressing the E_T and E_F with various parameters in Fig. 1.5 followed by differentiating with respect to V_{DG} , the depth of trap-detrap site (x_T) can be expressed as follows [11]:

$$x_T = \frac{T_{ox} \left[\frac{kT}{q} \frac{d \ln(\tau_c / \tau_e)}{dV_{DG}} - \frac{d|\psi_s|}{dV_{DG}} \right]}{1 - \frac{d|\psi_s|}{dV_{DG}}} \quad (1.2)$$

where T_{ox} is the oxide thickness and ψ_s is surface potential of drain region which is expressed in Ref. [11]. Energy level of trap-detrap site ($E_{Cox} - E_T$) can be also extracted using Eq. (1.1) and calculated x_T . In the Ref. 11, RTN in BTB GIDL current region was measured as shown in Fig. 1.7. Based on the above equations and extracted time constants with respect to V_{DG} , the depth and energy level of trap-detrap site causing GIDL current RTN could be extracted to 0.55 nm and 3.55 eV, respectively, as indicated Fig. 1.8 (a) and (b).

Also, capture cross section of trap-detrap site was extracted from the GIDL RTN measurement data. Time-domain RTN in BTB GIDL current was measured in conventional n-MOSFET as shown in Fig. 1.9 (a) [15]. In terms of hole trapping, time constants with respect to V_{DG} were extracted as indicated in Fig. 1.9 (b). These data were used to extract the depth and energy level of trap-detrap site. In addition, capture cross section of trap-detrap site (σ_c) could be extracted using the equation in inset of Fig. 1.9 (c).

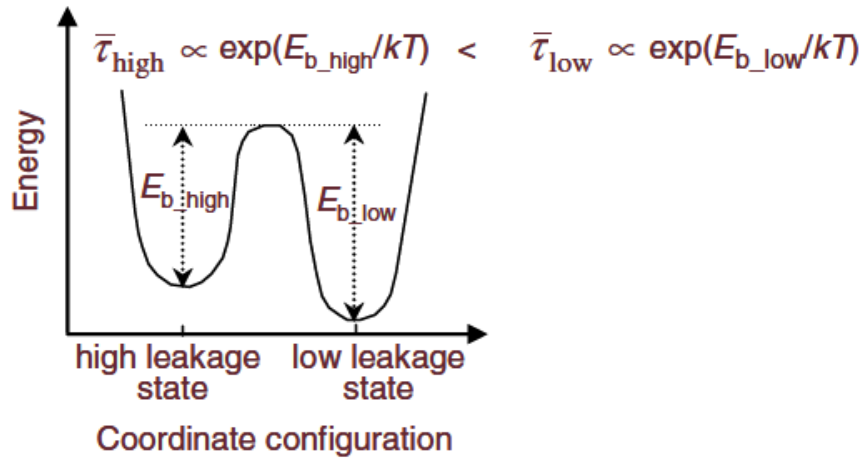


Fig. 1.3 Lattice configuration of bi-stable trap-detrap site causing RTN in junction leakage current (Yuki Mori et al., APL in 2010 [10])

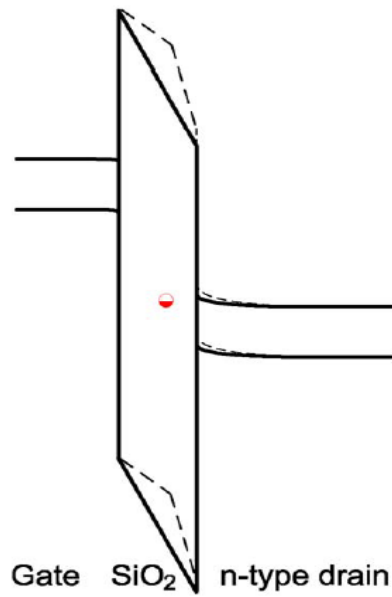


Fig. 1.4 Illustration on the electric field variation in energy band diagram with an electron capture into the trap-detrap site (Byoungchan Oh et al., TED in 2011 [11])

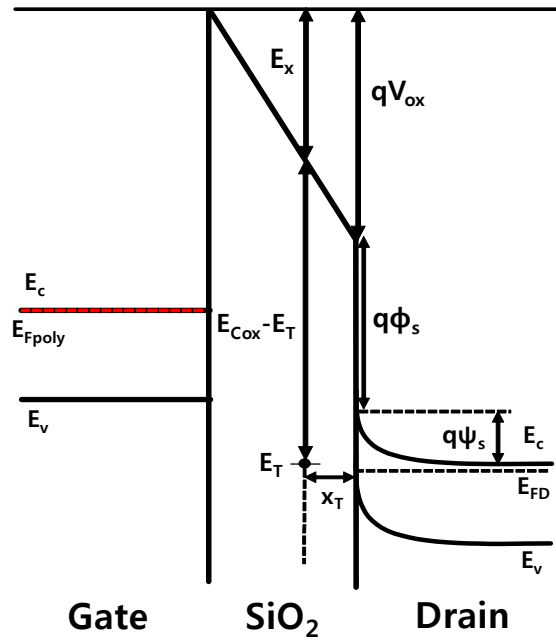


Fig. 1.5 Energy band diagram and related parameters in band-to-band tunneling GIDL current region (Byoungchan Oh et al., TED in 2011 [11])

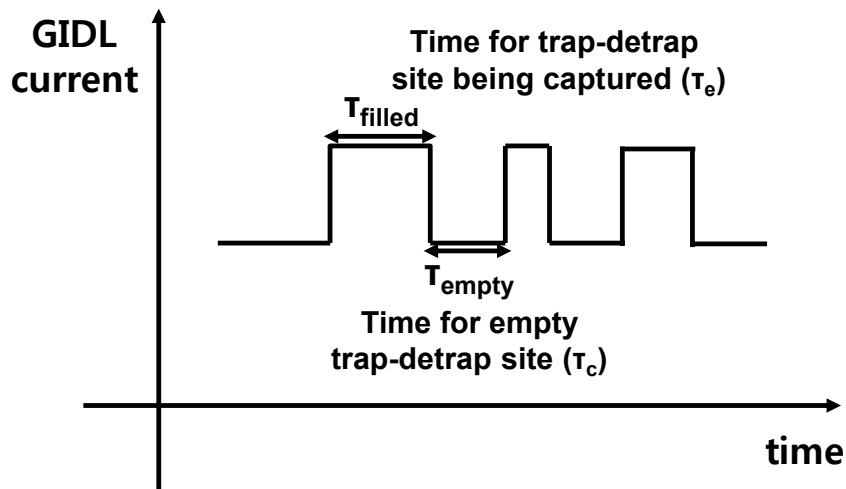


Fig. 1.6 The definition of τ_c and τ_e in time domain GIDL current RTN

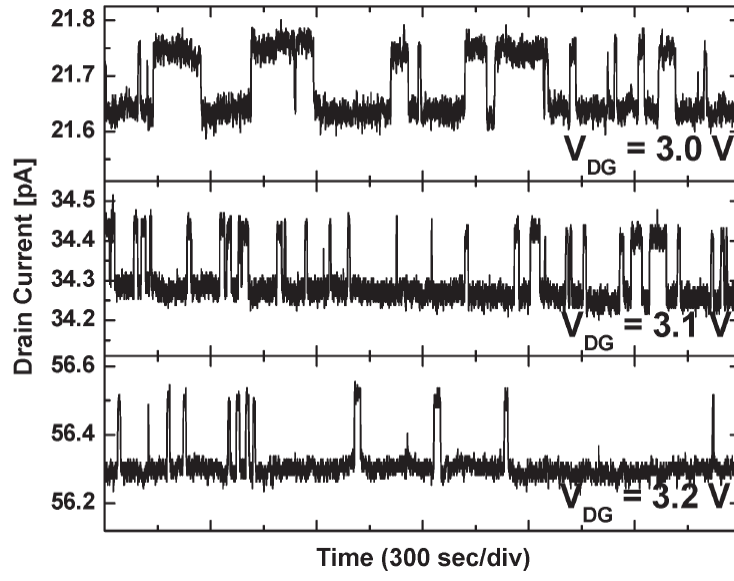


Fig. 1.7 Time domain RTN waveform in BTB GIDL current [11]

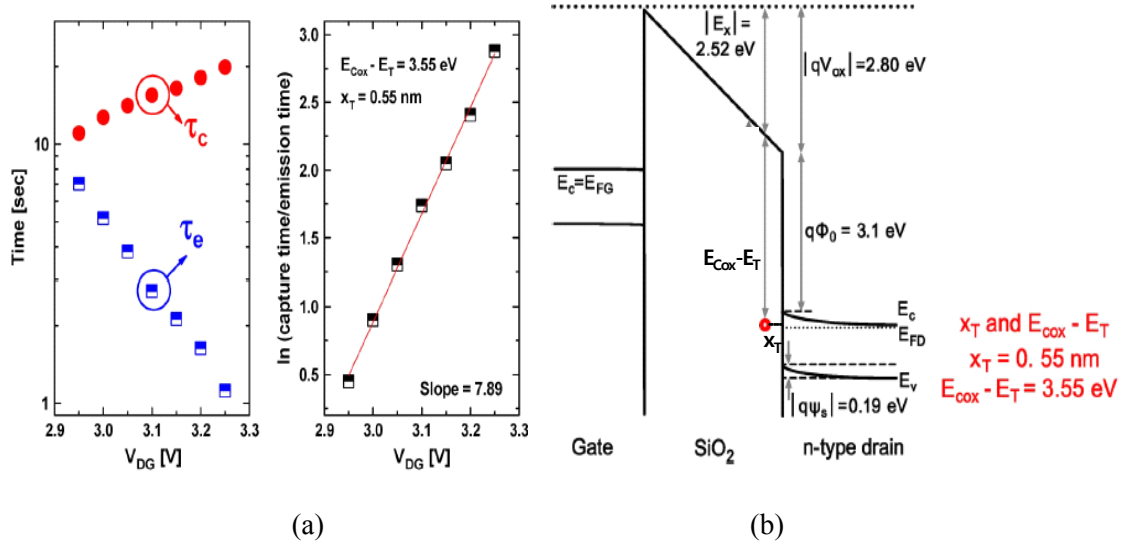


Fig. 1.8 (a) Variation of τ_c & τ_e , time constant ratio $\ln(\tau_c/\tau_e)$ and its linear slope with respect to V_{DG} and (b) extracted location of trap-detrap site in energy band diagram [11].

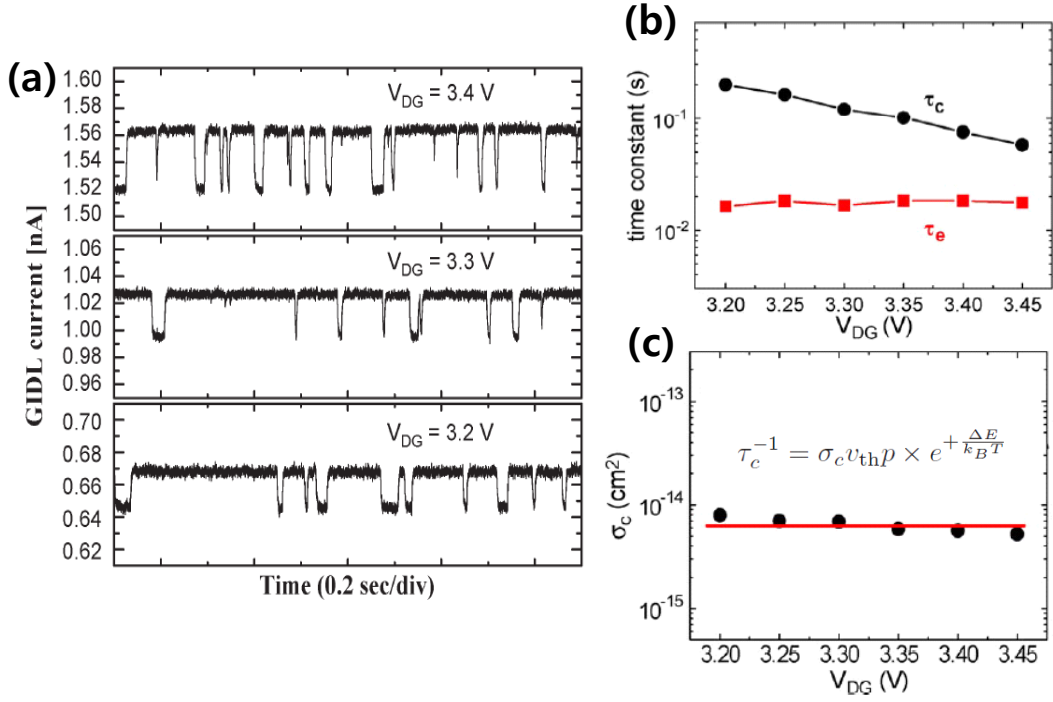


Fig. 1.9 (a) Measured time-domain RTN in BTB GIDL current with respect to V_{DG} , (b) extracted capture and emission time in terms of hole trapping and (c) capture cross section (σ_c) of GIDL RTN-induced trap-detrap site [15]

However, with device and supply voltage scaling (1.2 or 1.1 V supply voltage), GIDL current through trap-assisted tunneling (TAT) mainly flows in the low supply voltage region (or lower electric field region) as verified in Fig. 1.10. Fig. 1.10 shows the I_{GIDL} - V_D curves with various temperatures. In these curves, it is noted that there are weak V_D dependence on I_{GIDL} in 1.1-1.2 V of V_D . On the other hand, I_{GIDL} has strong temperature dependence in 1.1-1.2 V of V_D . This suggests that GIDL current mainly flows through trap-assisted tunneling (TAT) in this V_D range.

Fig. 1.11 (a) demonstrates the two trap sites (generation-recombination site (G-R site) and trap-detrap site) causing RTN in TAT GIDL current in energy band diagram of GIDL current region. Fig. 1.11 (b) also indicates above two trap sites in the cross-section view of planar MOSFET. As indicated in Fig. 1.11, two trap sites should be involved in order to occur RTN in TAT GIDL current unlike RTN in other current. The G-R site is just stepping-stone for the TAT GIDL current. From the charge-state fluctuation model, the current fluctuation was considered to be caused by the interaction between the trap-detrap site and G-R site [10]. Since two trap sites are involved for RTN in TAT GIDL current, more characteristics of trap sites should be analyzed. Thus, the researches on RTN in TAT GIDL current become important topics.

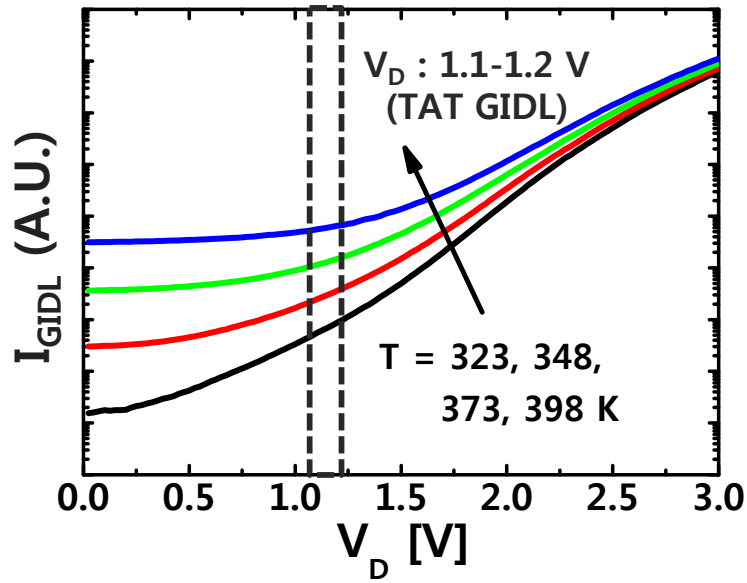


Fig. 1.10. I_{GIDL} - V_D curves with various temperatures.

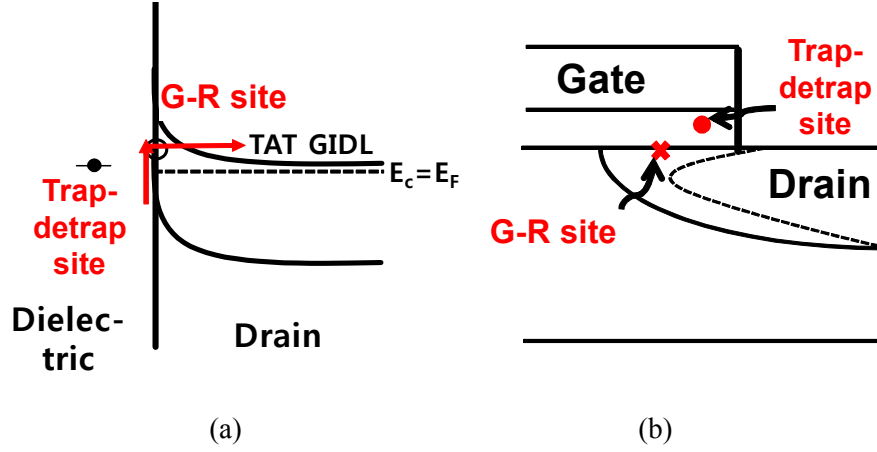


Fig. 1.11. Demonstrations on RTN in TAT GIDL current caused by two trap sites in (a) energy band diagram and (b) cross-section view of planar MOSFET.

There have been several researches on the RTN in TAT GIDL current in various literatures [16-18]. Most of the literatures, the TAT GIDL current in drain-to-substrate junction can be described as Hurkx's model based on the field enhancement factor $\Gamma(F)$ as follows:[19],[20]

$$I = I_{GR} [1 + \Gamma(F)] \propto \sigma \Gamma(F) \quad (\Gamma \gg 1) \quad (1.3)$$

$$\Gamma(F) = 2\sqrt{3\pi} \frac{F}{F_T} \exp \left[\left(\frac{F}{F_T} \right)^2 \right] \quad (1.4)$$

where I_{GR} is the thermal generation current via G-R site, σ is the capture cross-section of

the G-R site, F is the surface electric field at the G-R site, and F_r is a constant determined by the effective mass of an electron (m^*) which can be represented as follows:

$$F_r = \frac{\sqrt{24m^*(kT)^3}}{q\hbar} \quad (1.5)$$

where \hbar is reduced Planck constant, k is Boltzmann's constant and T is absolute temperature. The value of the electron effective mass ranges from $0.3m_0$ to $0.4m_0$ [21].

In addition to the characteristics of trap sites such as depth, energy level and capture cross section mentioned above, the distance between two trap sites is also important parameters for analyzing the RTN in TAT GIDL current. In order to extract distance between two trap sites causing RTN in TAT GIDL current, the equation for TAT GIDL current ratio before and after electron capture into the trap-detrap site should be accurately derived and utilized. Thus far, there are couple of researches on TAT GIDL current ratio before and after electron capture into the trap-detrap site [12],[17]. However, these researches have remained on the basic stage yet. Moreover, each research has been several weaknesses for accurately extracting the distance between two trap sites causing RTN in TAT GIDL current region. The various researches on TAT GIDL current ratio that have been conducted until now will be explained in this section.

As a first step, it was simply assumed that the direction of electric field variation (ΔF) due to electron capture in the trap-detrap site was parallel to that of electric field due to the drain-to-gate voltage, F_{empty} [17]. That is, the electric field at the G-R site when the

trap-detrap site is filled with electron (F_{filled}) is equal to F_{empty} plus ΔF . With this assumption, the ratio between the trap-assisted tunneling (TAT) current before and after electron capture in the trap-detrap site (I_{filled}/I_{empty}) can be represented as follows [17]:

$$\frac{I_{filled}}{I_{empty}} = \left(1 + \frac{\Delta F}{F_{empty}} \right) \exp\left(\frac{2F_{empty}\Delta F}{F_{\Gamma}^2} \right) \quad (1.5)$$

where F_{empty} is the electric field at the G-R site when the trap-detrap site is empty. ΔF is the modulation of electric field at the G-R site caused by electron occupancy into the trap-detrap site, which is equal to $q/4\pi\epsilon_{Si}r^2$. And, r is the distance between the two trap sites, ϵ_{Si} is the permittivity of Si, and x_T is the perpendicular distance between the trap-detrap site and the interface.

However, the direction of ΔF varies with the position of trap-detrap site despite of same distance between two trap sites. In general, the direction of ΔF is not parallel to that of F_{empty} as illustrated in Fig. 1.12. The method for F_{filled} derivation should be newly proposed as a further step.. Fig. 1.12 demonstrate cross section view of n-MOS transistor with two trap sites interacting with each other in case of empty trap-detrap site (Fig. 1.12 (a)) and trap-detrap site filled with electron (Fig. 1.12 (b)). In Ref. 23, F_{filled} was represented as vector summation of F_{empty} and ΔF . F_{filled} was derived using the 2nd cosine law as follows [18]:

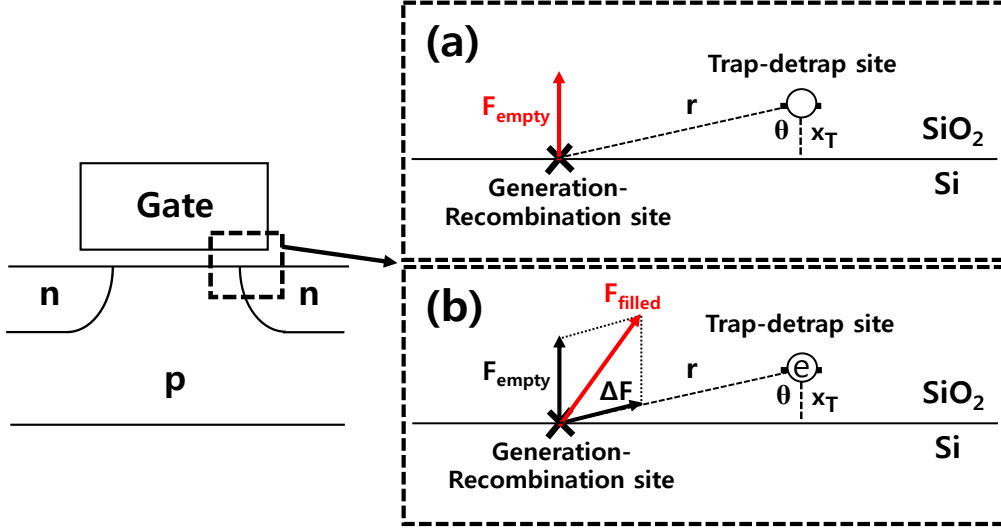


Fig. 1.12. Cross-section of n-MOS transistor with two trap sites interacting with each other in case of (a) empty trap-detrap site and (b) trap-detrap site filled with electron [18]

$$\cos(\pi - \theta) = \frac{(F_{empty})^2 + (\Delta F)^2 - (F_{filled})^2}{2F_{empty}\Delta F} \quad (1.6)$$

$$\therefore F_{filled} = \sqrt{(F_{empty})^2 + (\Delta F)^2 + 2F_{empty}\Delta F \frac{x_T}{r}}$$

On the contrast to the above result (Eq. (1.5)), capture cross section variation of G-R site with electron capture into the trap-detrap site ($\sigma_{filled}/\sigma_{empty}$) was considered in Ref. [18], which can be represented as follows [10]:

$$\frac{\sigma_{filled}}{\sigma_{empty}} = \exp\left(-\frac{q^2}{4\pi\epsilon_{Si}rkT}\right) \quad (1.7)$$

Based on the Eq. (1.3) and above results, I_{filled}/I_{empty} could be represented as the product of $\sigma_{filled}/\sigma_{empty}$ and field enhancement factor variation ($\Gamma_{filled}/\Gamma_{empty}$) as follows [18]:

$$\frac{I_{filled}}{I_{empty}} = \frac{\sigma_{filled}}{\sigma_{empty}} \frac{\Gamma_{filled}}{\Gamma_{empty}} \quad (1.8)$$

$$= \exp\left(-\frac{q^2}{4\pi\epsilon_{Si}rkT}\right) \frac{\sqrt{(F_{empty})^2 + \left(\frac{q}{4\pi\epsilon_{Si}r^2}\right)^2} + 2F_{empty}\left(\frac{q}{4\pi\epsilon_{Si}r^2}\right)\frac{x_T}{r}}{F_{empty}} \exp\left[\frac{q}{4\pi\epsilon_{Si}r^2F_{\Gamma}^2}\left(\frac{q}{4\pi\epsilon_{Si}r^2} + 2F_{empty}\frac{x_T}{r}\right)\right]$$

Fig. 1.13 plots I_{filled}/I_{empty} as a function of r with different x_T based on the Eq. (1.8). The point of intersection between Eq. (1.8) and I_{high}/I_{low} curve extracted from the measured time-domain RTN waveform corresponds to the distance between the two trap sites r .

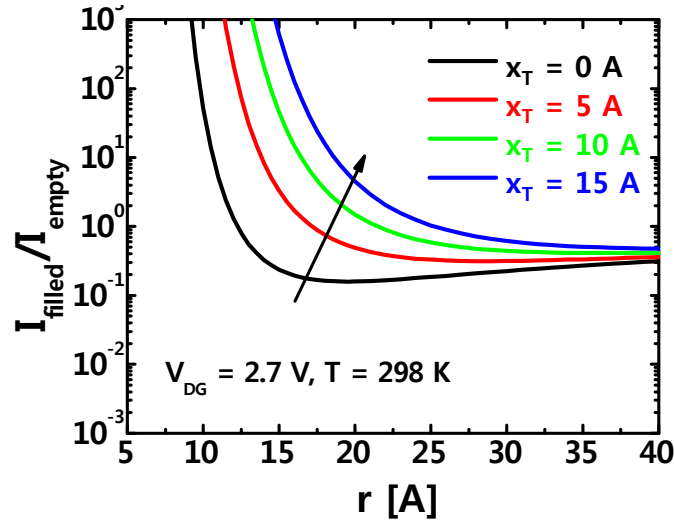


Fig. 1.13. The TAT current ratio before and after electron trapping (I_{filled}/I_{empty}) with various x_T as a function of r [18]

In Ref. [23], RTN in TAT GIDL current region was actually measured in n-type MOSFET. Fig. 1.14 (a) shows the measured GIDL current at 298 K with increasing the bias between the drain and the gate, V_{DG} . The ratio of τ_{low} to τ_{high} [$\ln(\tau_{low}/\tau_{high})$] and its linear slope with V_{DG} are also indicated in Fig. 1.14 (b). From the slope of the line, it can be known that the trap-detrap site causing RTN in TAT GIDL current was located at 0.7 Å from the Si/SiO₂ interface, which is essentially interface trap-detrap site [18].

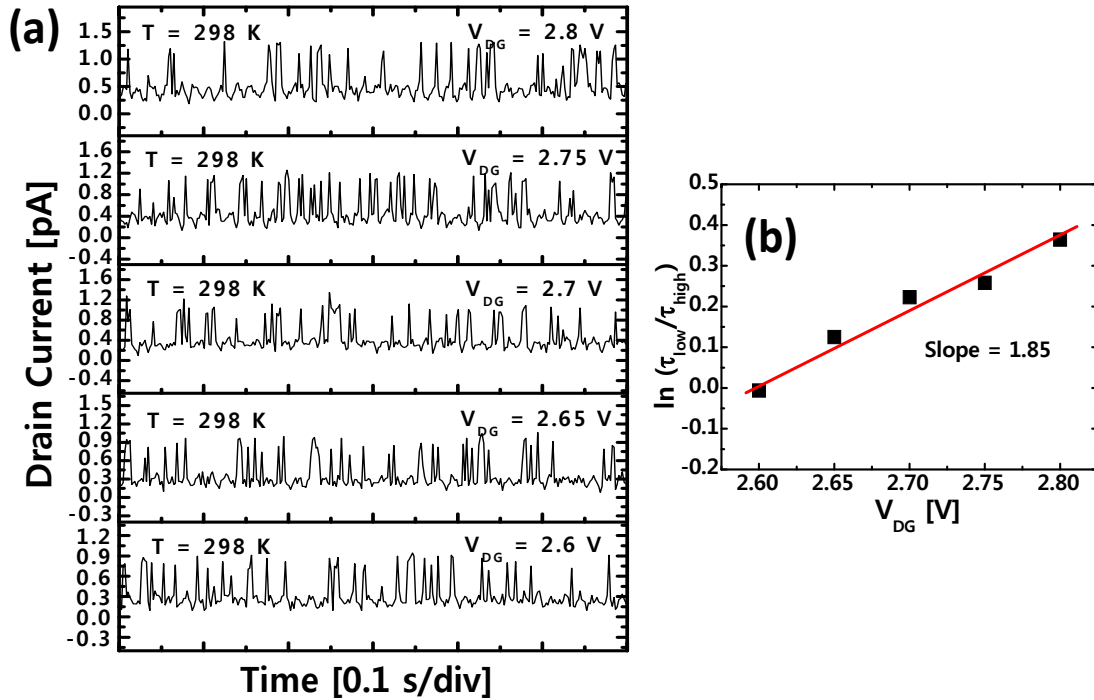


Fig. 1.14. (a) Measured time-domain GIDL current at 298 K with increasing V_{DG} and (b) Ratio of τ_{low} to τ_{high} [$\ln(\tau_{low}/\tau_{high})$] and its linear slope with increasing V_{DG} [18]

Fig 1.15 (a) showed the I_{filled}/I_{empty} value with V_{DG} measured from Fig. 1.14 (a). The measured current ratio between I_{filled} and I_{empty} was about 5.4 at $V_{DG} = 2.7$ V. Using the Fig. 1.13 and Fig. 1.15 (a), the distance between two trap sites r was extracted at each RTN-measured V_{DG} value in Ref. [18]. Fig 1.15 (b) showed the extracted distance between the two states at different V_{DG} values. In this figure, the extracted r value was almost constant for different V_{DG} values. This confirmed the validity of the extraction result. The extracted r value was 11.0 Å. If the fluctuation of the capture cross-section is ignored, the first term in the right-hand-side of Eq. (1.8) is not used in the extraction procedure and the extracted distance r would be about 16.5 Å, which indicates that about a 50% error can be made.

The extracted distance r was interpreted under the framework of an inter-atomic distance in the silicon interface lattice structure in case of interface trap-detrap site [18]. The interface trap sites at Si/SiO₂ are generally the dangling bonds of the un-passivated silicon atom at the interface. Fig. 1.16 showed the top view of the silicon lattice structure at (100) surface. Since the lattice constant of the silicon is 5.43 Å, the distance between atom A and atom B in the figure is 10.86 Å. From the above result, indicating that the extracted average r value is 11.0 Å, it could be concluded that the two trap sites at the two atom sites of A and B are possibly involved in RTN in TAT GIDL current [18].

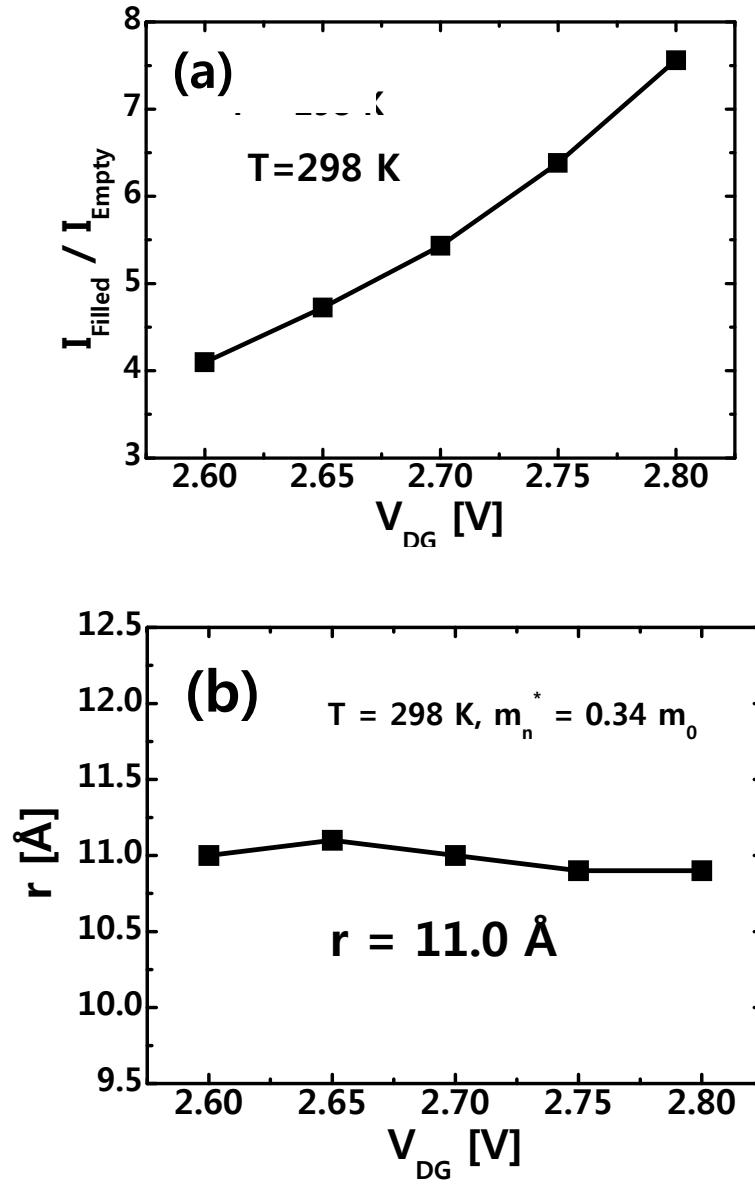


Fig. 1.15. (a) Measured current ratio ($I_{\text{filled}}/I_{\text{empty}}$) as a function of V_{DG} and (b) Extracted distance between the two interface trap sites (r) with V_{DG} [18].

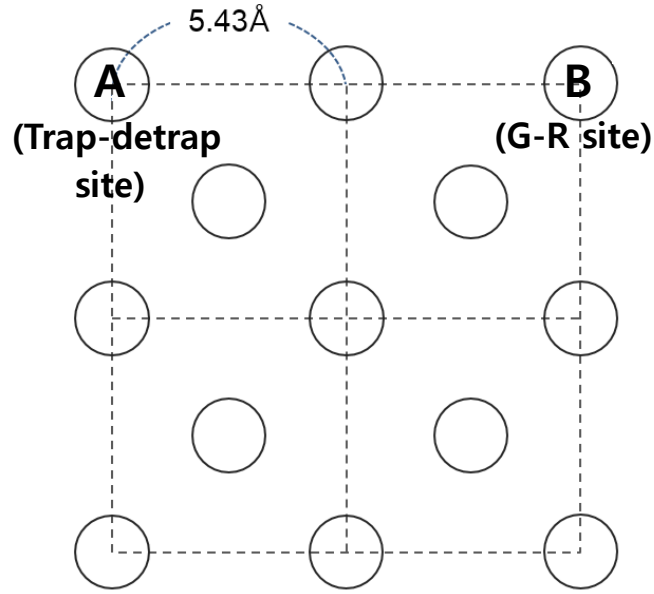


Fig. 1.16. Aerial view of silicon interface atom lattice structure [18]

However, this analysis still has weakness on accurately extracting the distance between two trap sites despite of many advances. In previous researches, the permittivity of silicon ϵ_{Si} has been simply used for the modulation of electric field at the G-R site ΔF caused by electron occupancy into the trap-detrap site although G-R site is located at silicon/dielectric interface [12],[18]. In fact, the permittivity of silicon and dielectric should be both considered for ΔF in electrostatics theory, which will be explained in this thesis.

Thus far, the characteristics of trap sites causing RTN in TAT GIDL current have been analyzed through various researches. However, it was not clearly determined how to occur RTN in GIDL current. That is, trapping mechanism into the trap-detrap site have

not been investigated. Also, the method for distinguishing possible trapping mechanism have not been proposed. Since trapping mechanism can provide the insight for understanding the physical characteristics of the trap sites, trapping mechanism should be clearly researched and determined.

In addition, the previous researches on RTN in TAT GIDL current has mainly focused on the drain/gate-interacted trap-detrap site located in dielectric and at interface based on charge state fluctuation model ((1) and (2) in Fig. 1.17). However, trap-detrap site inside drain region ((3) in Fig. 1.17) have a probability for causing RTN in TAT GIDL current. The parameters of trap sites in case of trap-detrap site inside drain region has not ever been extracted based on the charge state fluctuation model yet.

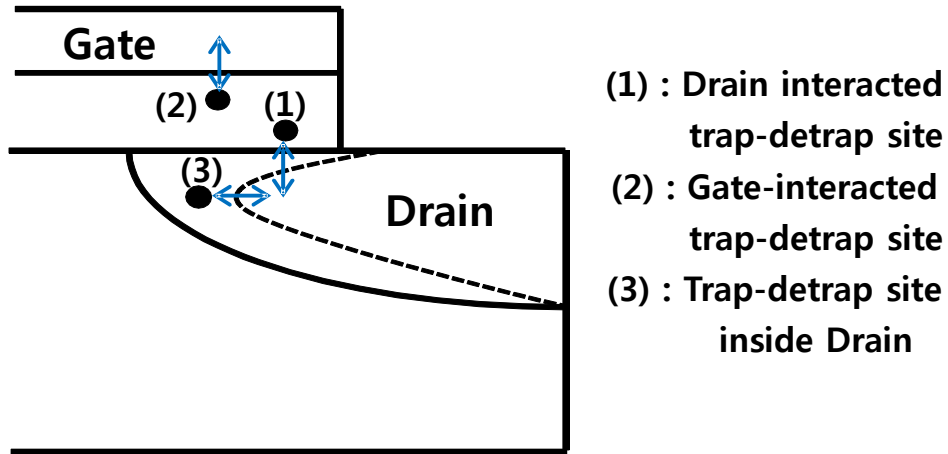


Fig. 1.17. The type of trap-detrap sites causing RTN in GIDL current.

In addition to the researches on the RTN in TAT GIDL current, the various device structures for access transistor in DRAM cell have been proposed. The requirements for access transistor are to minimize leakage current and increase on current. The conventional planar Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET) has limitations as very scaled DRAM cell transistor due to the short channel effect (SCE) which results in increase of leakage current.

In order to overcome the this limitation, recessed structure such as RCAT and SRCAT was proposed [22],[23]. This structure has been widely used and commercialized in DRAM manufacturing companies. Fig. 1.18 shows the cross-section view of RCAT and SRCAT structures. As shown in Fig 1.18, recessed structure has advantage of longer effective channel length (L_{eff}) and increase on gate controllability in same device demension. This feature results in the suppression of short channel effect (reduction of

leakage current). However, recessed structure has large gate-to-drain overlap region. This suggests that larger GIDL current flows through drain, which causes the retention time degradation in DRAM cell.

The Buried-Gate CAT (BCAT) structure was newly proposed in order to resolve this problems [24]. Fig. 1.19 shows the cross-section view of BCAT structure. The TiN metal gate is usually used. And, a part of TiN metal gate is etched below the silicon surface. These features makes the very short gate-to-drain overlap region which results in extremely small GIDL current and low resistive interconnect [24]. The researches on the GIDL current RTN in RCAT and SRCAT has been conducted [13]. However, GIDL current RTN in BCAT structure can't be measured easily and the studies on GIDL current RTN in this structure have rarely conducted.

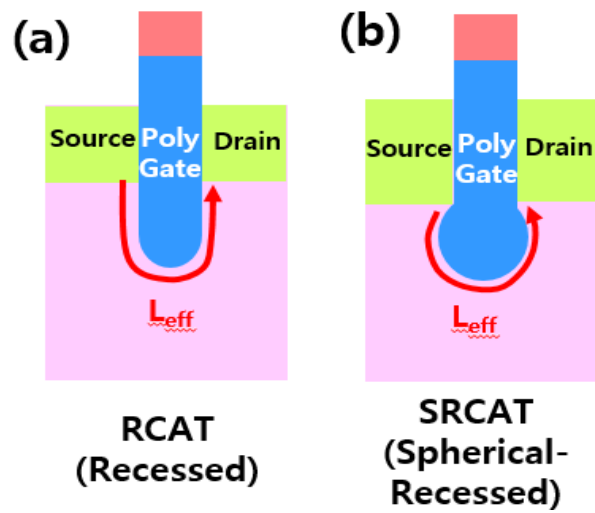


Fig. 1.18 The cross-section view of (a) RCAT and (b) SRCAT structures.

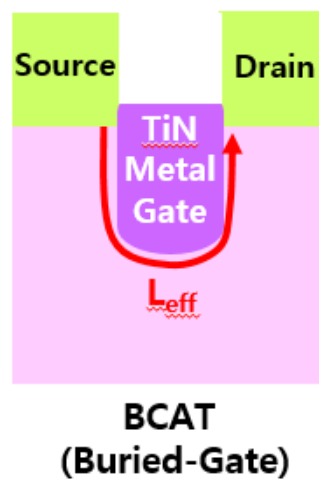


Fig. 1.19 The cross-section view of buried-gate CAT (BCAT) structure.

1.2 Scopes of thesis

In this thesis, the characteristics and trapping mechanism of trap sites (trap-detrap site generation-recombination site (G-R site)) in case of trap-detrap site inside dielectric or drain region causing Random Telegraph Noise (RTN) in Trap-assisted Tunneling (TAT) GIDL current were analyzed based on the RTN measurement in GIDL current and proposed equations. The several weaknesses and problems commented in introduction section are supplemented through various method in the thesis.

In chapter 2, RTN in TAT GIDL current in MOSFET was measured. Based on this measurement, analysis of two trap sites (G-R site and trap-detrap site) causing RTN in TAT GIDL current were conducted in case of trap-detrap site inside oxide. In addition, the effective permittivity of two different materials was used to accurately extract the distance between two trap sites causing RTN in TAT GIDL current.

In chapter 3, two possible trapping mechanisms were explained. And, trapping mechanism was determined based on the extracted activation energy of time constants in RTN in GIDL current with respect to temperature.

In chapter 4, trap-detrap site inside drain region causing RTN in TAT GIDL current was actually measured in BCAT for the first time. The equations for parameters related with the characteristics of trap sites were derived. Based on the equations and extraction methods, the characteristics of trap sites causing RTN in TAT GIDL current were extensively analyzed.

Chapter 2

The extraction of distance between two trap sites causing RTN in TAT GIDL current in case of oxide Trap-detrap site

In this chapter, measurement and analysis of two trap sites (G-R site and trap-detrap site) causing random telegraph noise (RTN) in trap-assisted tunneling (TAT) gate-induced drain leakage (GIDL) current were presented in case of trap-detrap site inside dielectric. In addition, the proper effective permittivity of two different materials was used to accurately extract the distance between two trap sites causing RTN in TAT GIDL current.

2.1 Introduction

Random telegraph noise (RTN) occurs when charges are randomly trapped and de-trapped from trap-detrap site that have an energy level within a few kT from the Fermi level and are located in the gate oxide or at Si/dielectric interface [25],[26]. Gate-induced drain leakage (GIDL) current mainly flows due to band-to-band (BTB) or trap-assisted tunneling (TAT), and it is the dominant leakage current component in dynamic random-access memory (DRAM) cells [27],[28]. RTN in the GIDL current has been reported to be the primary origin of the variable retention time phenomenon that significantly affects the retention characteristics of DRAM cell [9].

Recent studies on GIDL current RTN in the TAT region have been conducted, and the distance between two trap sites that cause RTN in TAT GIDL current was determined according to the current ratio between TAT GIDL current before and after electrons are captured in the trap-detrap site [17],[18].

However, previous studies suffered from a couple of drawbacks and limitations. First, the permittivity of silicon was only used to calculate the variation in the electric field instead of the effective permittivity [17],[18]. These disadvantages have resulted in an inaccurate extraction of the distance between two traps. Second, analyzed trap-detrap sites causing RTN in TAT GIDL current region were only located at the Si/dielectric interface. However, trap-detrap site inside dielectric can also cause the RTN in TAT GIDL current.

In this chapter, we characterized the trap sites that produced GIDL RTN in the TAT region in case of trap-detrap site inside dielectric. The proper effective permittivity for a variation in the electric field variation can be used to obtain the distance between two trap sites in a device in which the RTN is measured for an oxide trap-detrap site. These analyses provide a better understanding of the physical characteristics of trap sites causing RTN in a TAT GIDL current.

2.2 Measurement setup and Background

The devices used for this experiment consisted of a planar bulk n-MOSFET with a gate length of 280 nm (sample A) and 250 nm (sample B), a gate width of 10 μm , and a gate oxide thickness of 6.9 nm. Poly-silicon is used in the devices as the gate material, and the doping concentration of the source and drain is of $9 \times 10^{19} \text{ cm}^{-3}$. In contrast, the doping concentration of the substrate region is of $8.4 \times 10^{17} \text{ cm}^{-3}$.

Unlike drain current RTN, two trap sites are involved for RTN in TAT GIDL current as shown in Fig. 2.1. The generation-recombination site (G-R site) is just stepping-stone at the TAT GIDL current. The amplitude of electric field and capture cross section of G-R site is modulated with electron occupancy into the trap-detrap site, which results in the fluctuation of TAT GIDL current.

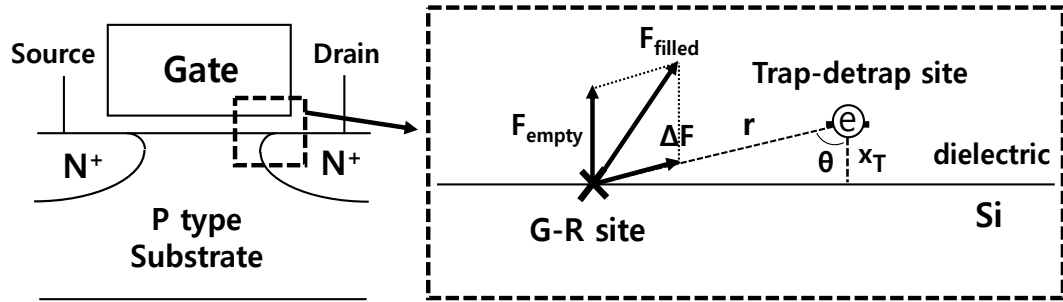


Fig. 2.1. Cross section of n-MOS transistor with two trap sites interacting with each other.

Fig. 2.2 (a) and (b) show the I_D - V_{DG} curves for the devices at 323K. Trap-assisted tunneling (TAT) can be seen to be dominant when the voltage applied between the drain and the gate V_{DG} = 4.4 V. Above that, a band-to-band tunneling current is dominant. Fig. 2.2 (c) and (d) show time-domain two-level RTNs during TAT GIDL current at a V_{DG} of 3.5–3.7 V (sample A) and 3.1–3.3 V (sample B) with 0.05 V intervals. The time constant ratio $[\ln(\tau_c/\tau_e)]$ is a function of V_{DG} can be extracted from the RTN measurement data in TAT GIDL current. From this value, the value of trap depth (x_T), which is the distance between the trap-detrap site and the interface, can be calculated by using Eq (1.2) [11].

The obtained depth (x_T) of each trap-detrap site are 0.55 nm in sample A and 0.68 nm in sample B, respectively. In addition, the activation energy (E_a) of the TAT current was measured at 0.60 eV in sample A and 0.54 eV in sample B, respectively. The equation for E_a of TAT current can be represented based on the Eq. (1.3) and (1.4) as follows [20]:

$$E_{a,TAT} = \frac{E_g}{2} + |E_t - E_i| - \frac{3}{2}kT - 3kT\left(\frac{F}{F_r}\right)^2 \quad (2.1)$$

This value ($E_{a,TAT}$) can be used to obtain the energy level of a G-R site (E_T - E_i) as indicated in Eq. (2.1) [20]. It can be known that the extracted E_a of the TAT current in each sample has relatively large value. This result can be explained as follows. The amount of energy band-bending at the drain is small in the TAT current (small F). Thus, the G-R site should be located far above the intrinsic level (E_i) for TAT being occurred. This means that the E_a of the TAT current is large. From the Eq. (2.1), the E_T - E_i values

were extracted to 0.16 eV and 0.11 eV, respectively.

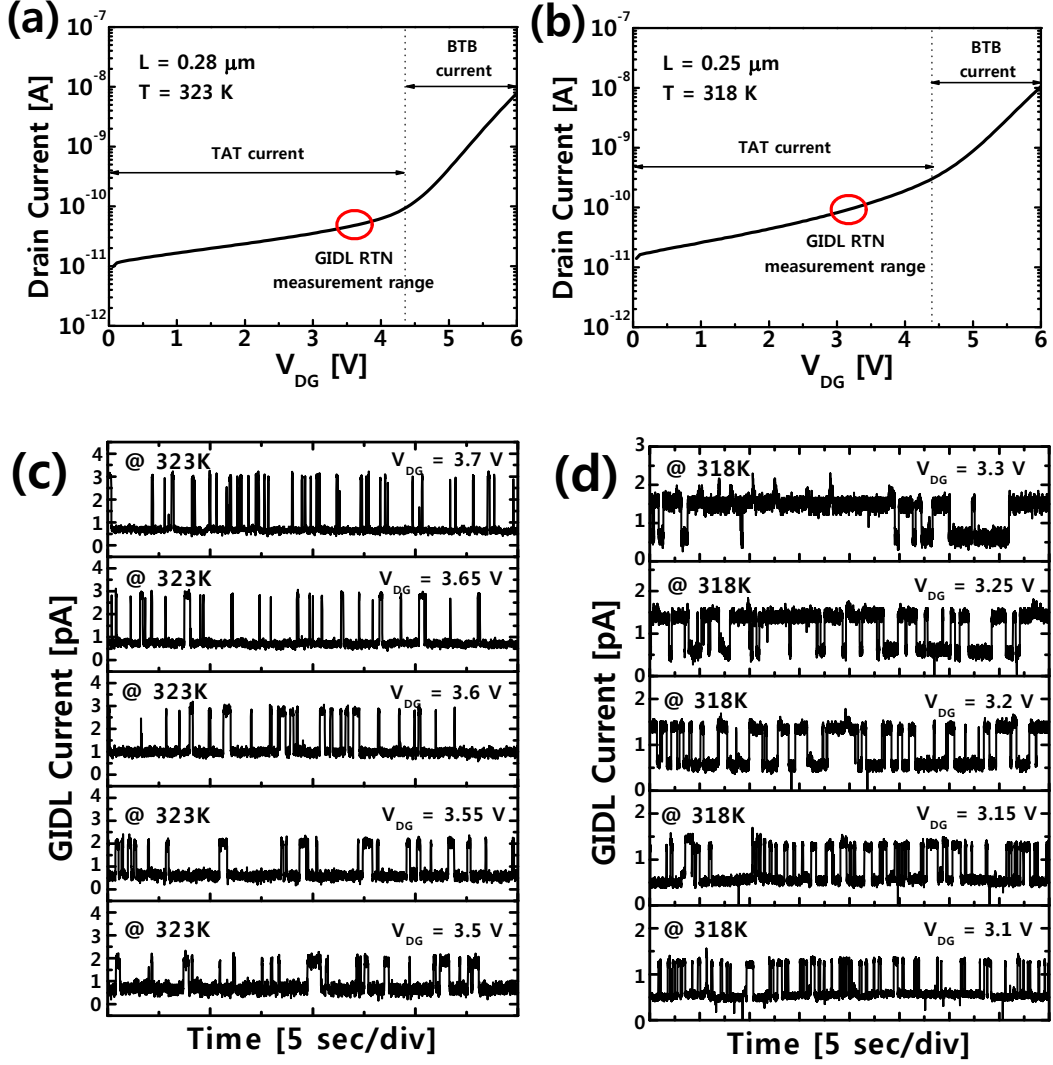


Fig. 2.2. I_D - V_{DG} curve for devices with RTN (a) at 323K with $W/L = 10/0.28$ μm (sample A) and (b) at 318K with $W/L = 10/0.25$ μm (sample B). Time-domain RTNs for a TAT GIDL current (c) at 323K (sample A) and (d) at 318 K (sample B) with an increase in V_{DG} .

Fig. 2.3 uses an energy band diagram to show the depths and the energy levels of the two trap sites in each sample. From this figure, it can be known that trap-detrap site in each sample is located in silicon dioxide and both G-R sites are acceptor-like trap as expected.

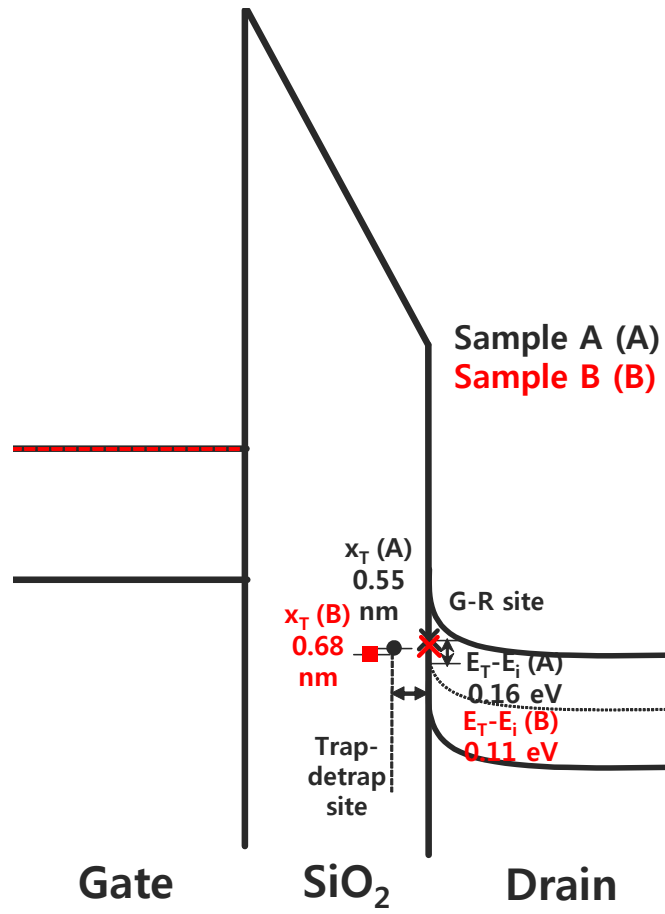


Fig. 2.3. The depths and energy levels of two trap sites in an energy band diagram of each sample.

2.3 Accurate extraction of the distance between two trap sites

The ratio between the TAT GIDL current before and after electron capture in the trap-detrap site (I_{filled}/I_{empty}) was determined by using the following equation for the interface of the trap-detrap site ($x_T = 0$) in Ref. [10], [18]:

$$\frac{I_{filled}}{I_{empty}} = \exp\left(-\frac{q^2}{4\pi\epsilon_{Si}rkT}\right) \frac{\sqrt{(F_{empty})^2 + \left(\frac{q}{4\pi\epsilon_{Si}r^2}\right)^2}}{F_{empty}} \exp\left[\left(\frac{q}{4\pi\epsilon_{Si}r^2F_{\Gamma}}\right)^2\right] \quad (2.2)$$

where I_{filled} and I_{empty} respectively represent the current levels when the trap-detrap site is filled with an electron and when it is empty. In this equation, ϵ_{Si} is the permittivity of silicon, r is the distance between the two trap sites, and F_{empty} is the electric field at the G-R site when the trap-detrap site is empty. However, contrary to the observations presented in Ref. [18], the effective permittivity ϵ_{eff} should be used to more accurately calculate I_{filled}/I_{empty} if the G-R site is located at the Si/SiO₂ interface [29], [30]. ϵ_{eff} is the effective permittivity and is equal to $(\epsilon_{Si} + \epsilon_{ox})/2$, and ϵ_{ox} is the permittivity of SiO₂. Based on the Fig. 2, the following equation can be derived using the 2nd cosine law:

$$\cos(\pi - \theta) = -\cos(\theta) = -\frac{x_T}{r} = \frac{(F_{empty})^2 + (\Delta F)^2 - (F_{filled})^2}{2F_{empty}\Delta F} \quad (2.3)$$

In this equation, F_{filled} is the electric field at the G-R site when the trap-detrap site is filled with electron. And, ΔF is the modulation of electric field at the G-R site caused by electron occupancy into the trap-detrap site, which is equal to $q/4\pi\epsilon_{eff}r^2$. To verify this explanation, Fig. 2.4 plots simulation data of ΔF versus r in planar bulk n-MOSFET having same dimension with sample A [31]. And, the ΔF equations in case of $q/4\pi\epsilon_{eff}r^2$ and $q/4\pi\epsilon_{Si}r^2$ are also plotted with the simulation data of ΔF versus r . As indicated in Fig. 2.4, the simulation data of ΔF is well fitted with ΔF which is equal to $q/4\pi\epsilon_{eff}r^2$. From the Eq. (2.3), F_{filled} can be represented as the following equation:

$$F_{filled} = \sqrt{(F_{empty})^2 + \left(\frac{q}{4\pi\epsilon_{eff}r^2}\right)^2 + 2F_{empty}\left(\frac{q}{4\pi\epsilon_{eff}r^2}\right)\frac{x_T}{r}} \quad (2.4)$$

Therefore, I_{filled}/I_{empty} can be expressed as the following equation for the case of an oxide trap-detrap site ($x_T \neq 0$):

$$\begin{aligned}
& \frac{I_{filled}}{I_{empty}} \\
& = \exp\left(-\frac{q^2}{4\pi\epsilon_{eff}rkT}\right) \sqrt{\frac{(F_{empty})^2 + \left(\frac{q}{4\pi\epsilon_{eff}r^2}\right)^2 + 2F_{empty}\left(\frac{q}{4\pi\epsilon_{eff}r^2}\right)\frac{x_T}{r}}{F_{empty}}} \exp\left[\frac{q}{4\pi\epsilon_{eff}r^2F_1^2}\left(\frac{q}{4\pi\epsilon_{eff}r^2} + 2F_{empty}\frac{x_T}{r}\right)\right] \\
& \quad (2.5)
\end{aligned}$$

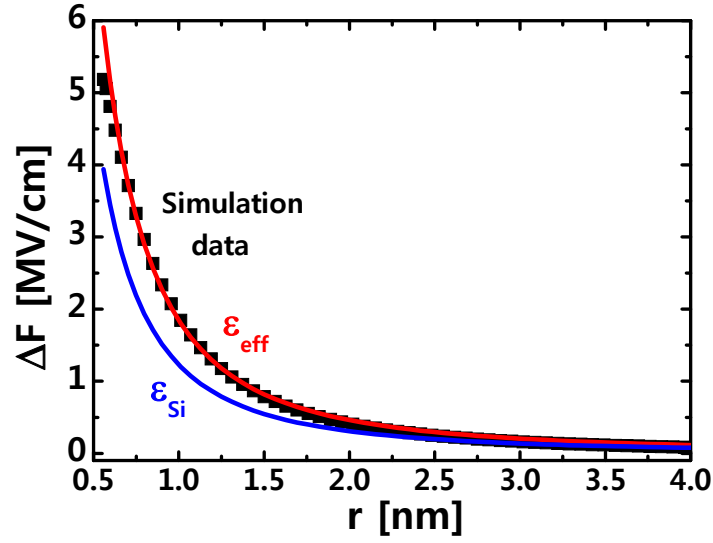


Fig. 2.4. Simulation data of ΔF and ΔF equations in case of $q/4\pi\epsilon_{eff}r^2$ and $q/4\pi\epsilon_{Si}r^2$ versus r .

2.4 Results and Discussion

Fig. 2.5 (a) and (b) shows the I_{filled}/I_{empty} ratio against V_{DG} in sample A and B,

respectively. I_{filled} and I_{empty} respectively represent the current levels when the trap-detrap site is filled with an electron and when it is empty. The I_{filled}/I_{empty} value can be used to determine the distance between the two trap sites (r). Fig. 2.6 (a) shows the plots for Eq. (2.5) and for the I_{filled}/I_{empty} value obtained in Fig. 2.5 (a) when $V_{DG} = 3.6$ V, $T = 323$ K, and $x_T = 0.55$ nm (sample A). The point of intersection between the two curves corresponds to the distance between the two trap sites, which is 1.71 nm in this case. Fig. 2.6 (b) shows the r value with respect to V_{DG} . If ϵ_{si} were used as the permittivity for the ΔF instead of ϵ_{eff} , the r value would be 1.54 nm, which indicates that an error of about 9.9 % was made.

Fig. 2.7 shows the cross-section of the positions of the two trap sites in the gate-to-drain overlap region. The x_T and r values extracted from Fig. 2.13 and 2.15 can be used to accurately determine the relative positions of the trap sites causing RTN in the TAT GIDL current.

The distance between the two trap sites (r) can be also extracted using similar manner in case of sample B. Fig. 2.8 (a) shows the plots for Eq. (2.5) and for the I_{filled}/I_{empty} value obtained in Fig. 2.5 (b) when $V_{DG} = 3.2$ V, $T = 318$ K, and $x_T = 0.68$ nm (sample B). The point of intersection between the two curves corresponds to the distance between the two trap sites, which is 1.59 nm in this case.

Fig. 2.9 shows the cross-section of the positions of the two trap sites in the gate-to-drain overlap region. The extracted x_T and r values can be also used to accurately determine the relative positions of the trap sites causing RTN in the TAT GIDL current.

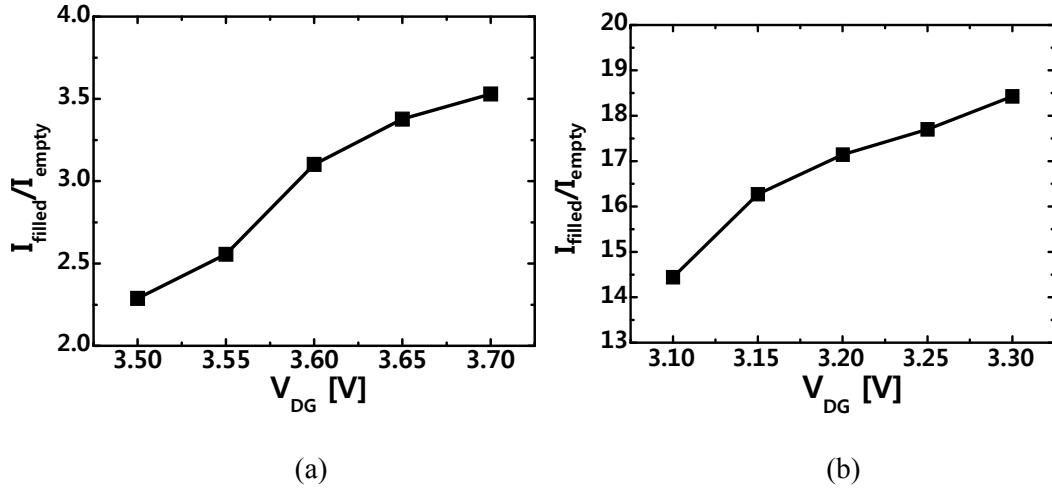


Fig. 2.5. Measured $I_{\text{filled}}/I_{\text{empty}}$ with respect to V_{DG} in (a) sample A and (b) sample B

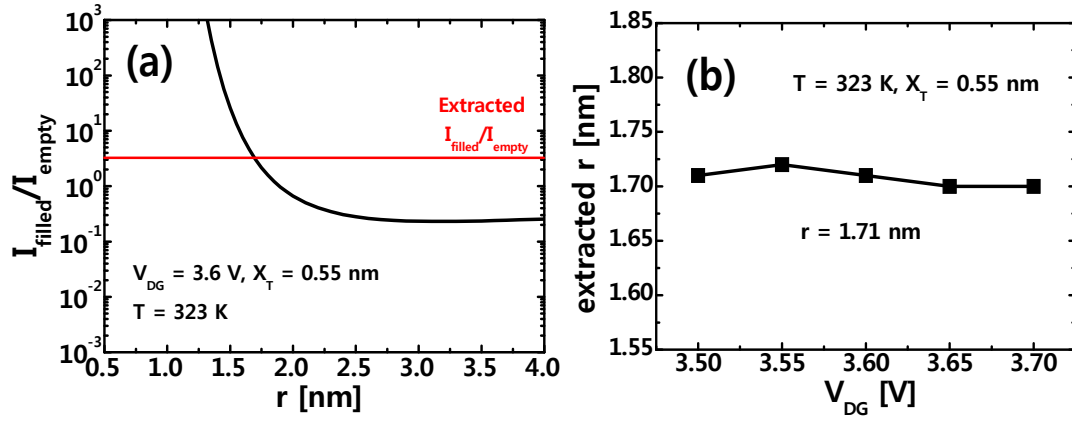


Fig. 2.6. (a) $I_{\text{filled}}/I_{\text{empty}}$ value and $I_{\text{filled}}/I_{\text{empty}}$ extracted from Fig. 2.5 (a) with respect to r and (b) r extracted with V_{DG} when $T=323$ K and $x_{\text{T}}=0.55$ nm (sample A)

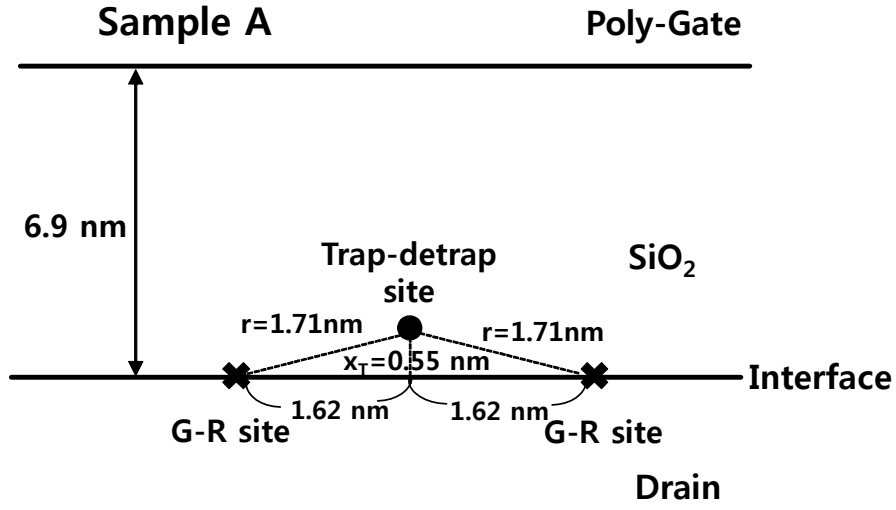


Fig. 2.7. Illustration of the distance between two trap sites based on the results shown in Fig. 2.6 (b). ($V_{DG} = 3.6$ V in sample A)

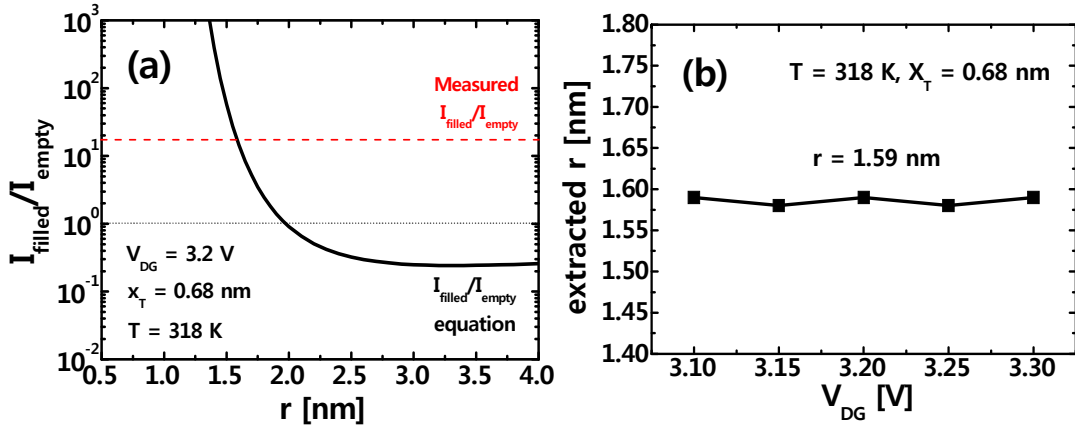


Fig. 2.8. (a) I_{filled}/I_{empty} value and I_{filled}/I_{empty} extracted from Fig. 2.5 (b) with respect to r and (b) r extracted with V_{DG} when $T=318$ K and $x_T=0.68$ nm (sample B)

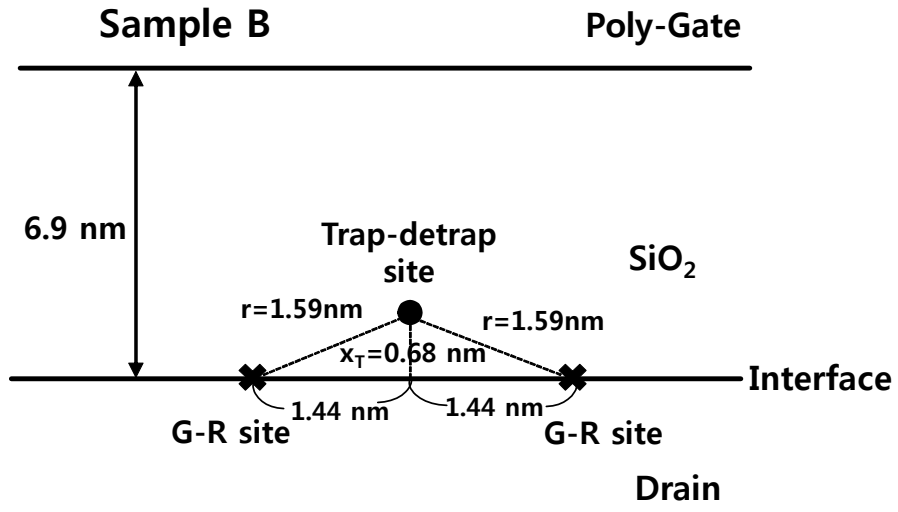


Fig. 2.9. Illustration of the distance between two trap sites based on the results shown in Fig. 2.8 (b). ($V_{DG} = 3.2 \text{ V}$ in sample B)

2.5 Summary

The RTNs in TAT GIDL current caused by oxide trap-detrap site were actually measured in n-MOSFET transistor. The two trap sites (G-R site and trap-detrap site) that cause RTN during TAT GIDL current were physically characterized. And, the distance between the two trap sites causing RTN in TAT GIDL current was accurately determined for the oxide trap-detrap site by making proper use of the effective permittivity of two different materials.

Chapter 3. Analysis on Trapping Mechanism of Trap-detrap site Causing GIDL Current RTN

3.1 Introduction

Gate-induced drain leakage (GIDL) current is most dominant leakage component in DRAM cell [21]. And, random telegraph noise (RTN) in GIDL caused by trap-detrap sites in the overlap region between gate and drain has been considered as the origin of variable retention time (VRT) phenomenon in DRAM cell. Thus, various researches on the GIDL RTN have been conducted [11],[15]. However, the accurate analysis on trapping mechanism of GIDL RTN has not been implemented yet. In this chapter, GIDL RTN with different V_{DG} and temperature was characterized. From these data, we extracted the physical parameters of trap-detrap site causing GIDL RTN. And, we determined the trapping mechanism based on activation energy comparison of capture and emission time.

3.2 Results and Discussion

We measured 2-level GIDL RTN in the planar n-type MOSFET with W/L of 0.5/0.12 μm and SiO_2 thickness of 3.7 nm. And, we characterized GIDL RTN with respect to V_{DG}

and temperature, while the gate, source and body bias were fixed to 0 V in order to neglect the other leakage components except GIDL current. Fig. 3.1 (a) shows measured time-domain GIDL RTN data with increasing V_{DG} at room temperature. From this figure, capture time (τ_c) and emission time (τ_e) were extracted. The τ_c , τ_e variation with V_{DG} is plotted in Fig. 3.1 (b). The ratio of τ_c to τ_e ($\ln(\tau_c/\tau_e)$) and its linear slope with V_{DG} are also indicated in Fig. 3.1 (c). Based on these results, we can extract the depth (x_T) & energy level ($E_{cox}-E_T$) of the trap-detrap site [11].

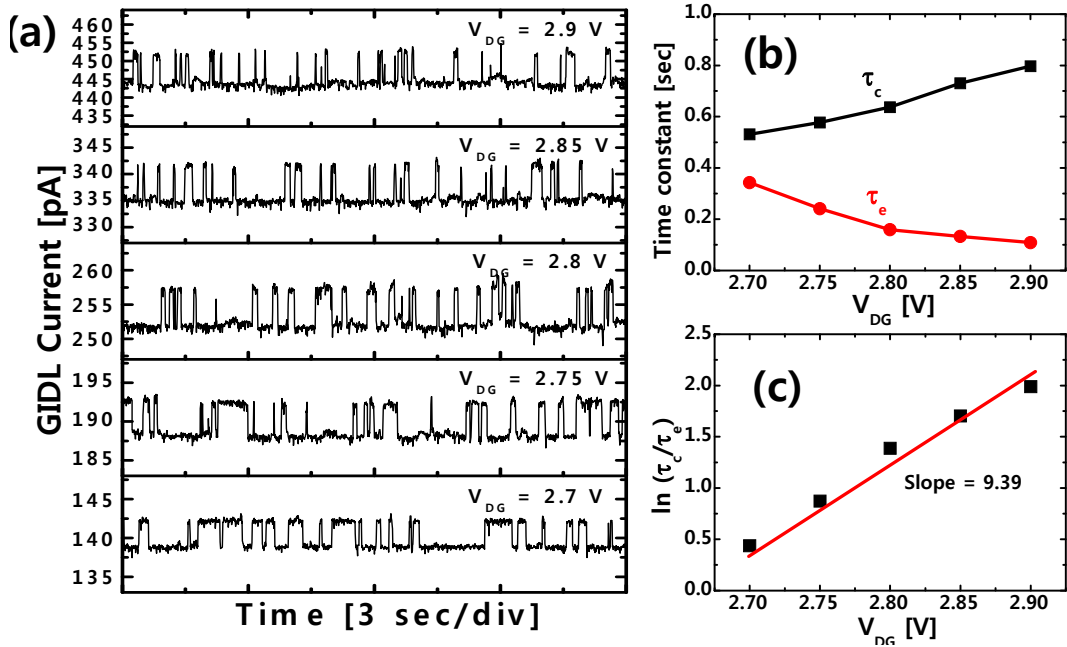


Fig. 3.1 (a) Measured time-domain data of GIDL RTN, (b) capture time (τ_c) and emission time (τ_e) variation, and (c) the ratio of τ_c to τ_e ($\ln(\tau_c/\tau_e)$) and its linear slope with V_{DG} for the sample ($W/L = 0.5/0.12 \mu\text{m}$, $T_{ox} = 3.7 \text{ nm}$).

Fig. 3.2 depicts x_T and $E_{Cox}-E_T$ of trap-detrap site causing GIDL current RTN at the energy diagram. The x_T and $E_{Cox}-E_T$ value are 0.03 nm and 3.45 eV with N_d of $4.1 \times 10^{19} \text{ cm}^{-3}$, respectively. The trap-detrap site can be interpreted as interface trap-detrap site. Fig. 3.3 (a) shows the measured time-domain GIDL current RTN at the constant V_{DG} ($V_{DG} = 2.7 \text{ V}$) with temperature. Time constants (capture time (τ_c) and emission time (τ_e)) can be represented as exponential dependence of below equation:

$$\tau = \tau_0 \exp\left(\frac{E_a}{kT}\right) \quad (3.1)$$

where τ_0 is the pre-factor, k is Boltzmann's constant, T is absolute temperature, and E_a is activation energy value of time constants. The activation energy value E_a of time constants can be extracted through the linear slope with $1/kT$ in Arrhenius plot. Fig. 3.3 (b) shows Arrhenius plot of τ_c and τ_e . The each activation energy value of τ_c and τ_e was indicated in the inset of Fig. 3.3 (b). It can be noted that the activation energy of τ_c is larger than that of τ_e in this sample, which will be utilized for determining the trapping mechanism.

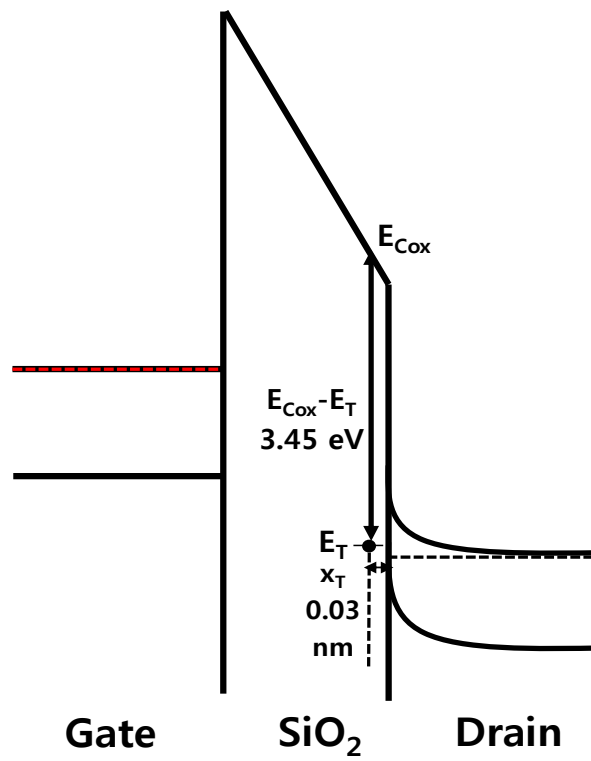


Fig. 3.2. The depth (x_T) and energy level ($E_{Cox} - E_T$) of trap-detrapped site causing GIDL RTN

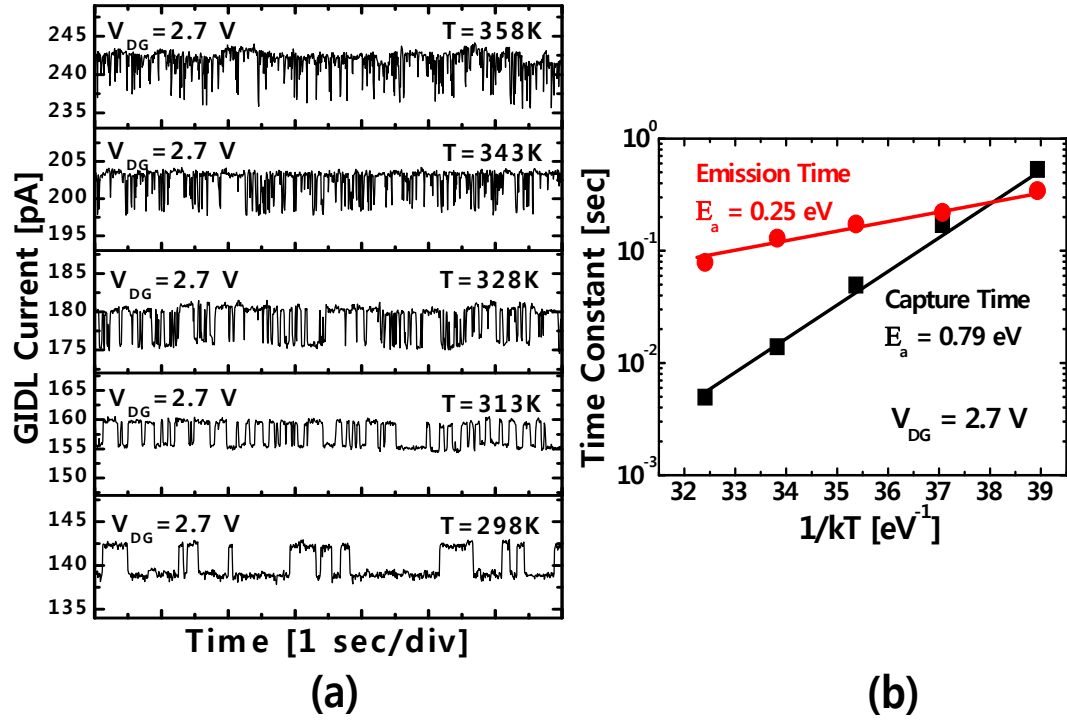


Fig. 3.3 (a) Time-domain GIDL RTN data at $V_{DG}=2.7 \text{ V}$ with various temperature, and (b) Arrhenius plot of time constants and activation energy (E_a) of capture & emission time.

Fig. 3.4 (a) shows the time domain for the RTN measured in the TAT GIDL current with various temperatures at a constant value of V_{DG} ($V_{DG} = 3.55$ V) (in sample A of chapter 2). Fig. 3.4 (b) shows Arrhenius plots for τ_c and τ_e . E_a value can be extracted using similar manner applied in Fig. 3.3 (b). The E_a value for τ_c (0.10 eV) is smaller than that for τ_e (0.13 eV) on the contrary to the Fig. 3.3. In Fig. 3.3 and 3.4, charge trapping is generally possible with either electron trapping from conduction band (mechanism 1) or valence band (mechanism 2).

Fig. 3.5 illustrates the two possible mechanisms for electron trapping from conduction band (Fig. 3.5 (a)) and valence band (Fig. 3.5 (b)). As compared the energy level of trap-detrap site, conduction band and valence band in Fig. 3.5, mechanism 1 occurs if E_a of capture time is smaller than E_a of emission time. On the other hand, mechanism 2 occurs under the condition that E_a of capture time is larger than E_a of emission time. τ_c at each trapping mechanism with consideration of tunneling probability can be calculated using the equations in TABLE 3.1 [12]. As indicated in Fig. 3.3. (b), E_a of τ_c is 0.79 eV and $E_a(\tau_c)$ is larger than $E_a(\tau_e)$. In addition, surface potential (ψ_s) at $V_{DG}=2.7$ V is -0.353 V. This implies that it is impossible to explain the electron trapping through mechanism 1. Instead, mechanism 2 is appropriate mechanism to explain the trapping mechanism. And, $|E_B|$ and E_t-E_v can be calculated from the extracted parameters, which has values of 0.013 eV and 0.78 eV at $V_{DG}=2.7$ V & 298 K, respectively [32].

On the other hand, because the activation energy value for τ_c (0.10 eV) is smaller than that for τ_e (0.13 eV) and surface potential (ψ_s) at $V_{DG}=3.55$ V is -0.099 V in case of Fig. 3.

4, electron trapping mechanism of Fig. 3.4 can be explained by trapping from conduction band instead of valence band (mechanism 1) [33].

Fig. 3.6 (a) and (b) illustrate the lattice coordinate reconfiguration of electron trap-detrap site in case of Fig. 3.3 and Fig. 3.4 based on the determined trapping mechanism.

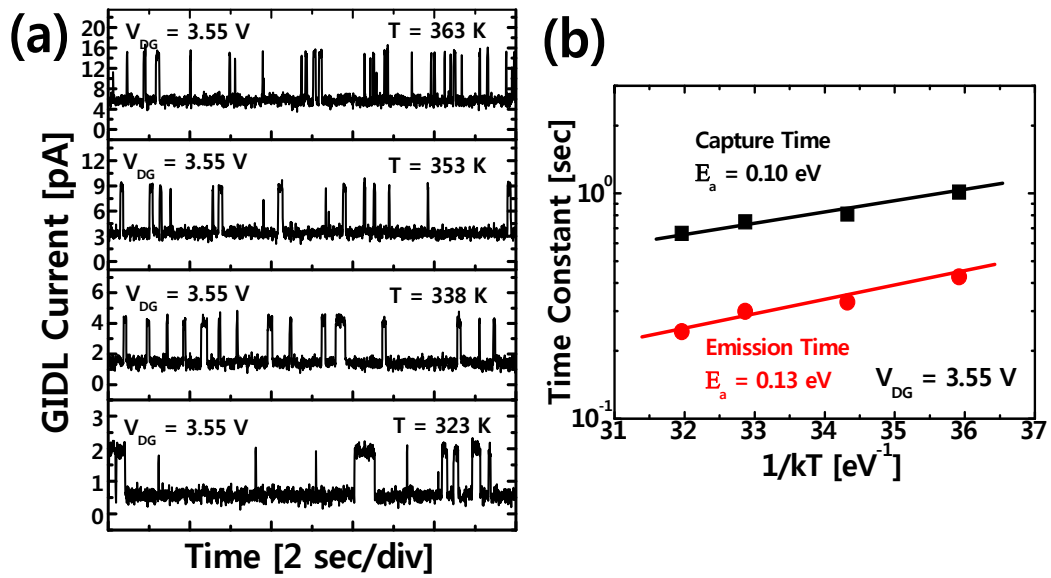


Fig. 3.4. (a) Measured time-domain of TAT GIDL RTN when $V_{DG} = 3.55$ V, and (b) τ_c and τ_e time constants with an increase in temperature. The activation energy values of τ_c and τ_e are also indicated in the inset of Fig. 3.4 (b).

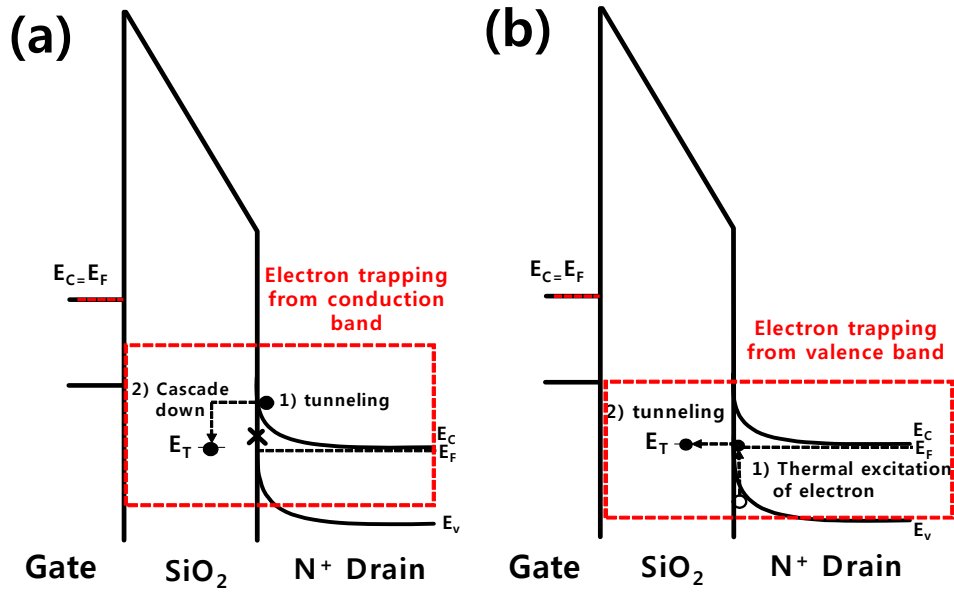


Fig. 3.5. Illustrations on two possible electron trapping mechanism: electron trapping (a) from conduction band (mechanism 1) and (b) valence band (mechanism 2).

TABLE 3.1. The equation for capture time with consideration of tunneling probability in case of mechanism (a) 1 and (b) 2.

	Capture time (τ_c)
Mechanism 1	$\tau_0 \exp\left[\frac{E_a}{kT}\right] = \frac{1}{R_s \times R_{e_tunnel}} \quad (a)$ $= \frac{2 \exp\left[\frac{2 \times T \sqrt{2 m_e^* (qV_{bar_c})}}{\hbar}\right]}{v_{thx_n} N_d \sigma} \exp\left[\frac{-q\psi_s}{kT}\right]$
Mechanism 2	$\tau'_0 \exp\left[\frac{ E_a }{kT}\right] = \frac{1}{R_{thr} \times R_{e_tunnel}} \quad (b)$ $= \frac{2 \exp\left[\frac{2 \times T \sqrt{2 m_e^* (qV_{bar_c})}}{\hbar}\right]}{v_{thx_p} N_v \sigma_{oc}} \exp\left[\frac{ E_B + (E_t - E_v)}{kT}\right]$

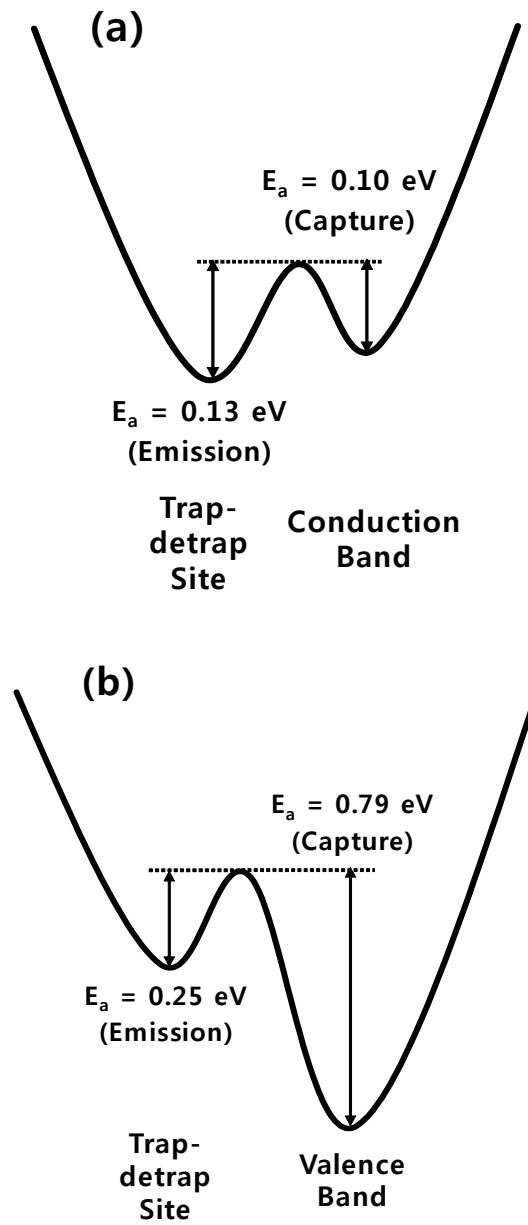


Fig. 3.6. Lattice coordinate reconfiguration of the electron trap-detrap site in case of (a)

Fig. 3.3 and (b) Fig. 3.4.

3.3 Summary

The GIDL current RTN with variation to V_{DG} and temperature was measured and analyzed. Through time constants variation with V_{DG} , the depth and energy level of trap-detrap site could be extracted. The larger activation energy value of τ_c extracted from the GIDL RTN data with temperature suggests that electron trapping occurs from the valence band, whereas the smaller activation energy value of τ_c suggests the electron trapping from conduction band. The GIDL current RTN which occurred by electron trapping from conduction band was for the first time measured in planar n-MOSFET. These analyses provide the insight for understanding the trapping mechanism of the trap-detrap site.

Chapter 4

Measurement and Analysis on Trap sites causing RTN during TAT GIDL current in case of Trap-Detrap site inside Drain region

In this chapter, trap-detrap site inside silicon region (drain region) causing RTN in trap-assisted tunneling (TAT) gate-induced drain leakage (GIDL) current was actually measured in Buried cell array transistor (BCAT) for the first time. From above measurement and derived equation in above chapters, the parameters related with the characteristics of trap-detrap and generation-recombination (G-R) site were extracted and comprehensively analyzed.

4.1 Introduction

Recently, buried-gate CAT (BCAT) structure has been used as DRAM cell transistor instead of recessed structure [34]. Conventional recessed structure has several advantages of large degree of integration and short channel effect suppression due to the increase in effective channel length. However, recessed structures such as RCAT and SRCAT have relatively large gate-to-drain overlap length. This fact causes larger GIDL current (or

leakage current). Instead, BCAT structure has additional advantage of very short overlap length between gate and drain region, which results in extremely small GIDL current. This results from the fact that a part of TiN metal gate is etched below the silicon surface as indicated in Fig. 1.6.

Gate-induced drain leakage (GIDL) current mainly flows due to band-to-band (BTB) or trap-assisted tunneling (TAT), and it is the dominant leakage component of current in dynamic random-access memory (DRAM) cells [27]. RTN in the GIDL current has been reported to be the primary origin of the variable retention time (VRT) phenomenon that significantly affects the retention characteristics of DRAM cells [9]. Until now, the researches on GIDL RTN have been focused on the trap-detrap site in the dielectric and silicon/dielectric interface. However, trap-detrap site inside silicon region (drain) can cause the RTN in GIDL current occasionally. Even though, the researches and methodology for analyzing the characteristics of trap-detrap site inside silicon region has been rarely conducted.

In this chapter, trap-detrap site inside drain region causing RTN in TAT GIDL current was actually measured in BCAT for the first time. Finally, the physical parameters related with the characteristics of trap-detrap and generation-recombination (G-R) site were extracted and analyzed through derived equations and methodologies mentioned in above chapters.

4.2 The depth and energy level of trap-detrap site inside drain region

Previous researches reported that the RTN in TAT GIDL current occurs due to the trap-detrap site inside dielectric or at interface [17-18, 33]. In fact, trap-detrap site inside drain region also causes the RTN in TAT GIDL current as shown in Fig. 4.1. However, this trap-detrap site could not be distinguished from the trap-detrap site inside dielectric or at interface. In addition, this trap-detrap site type have not been measured in RCAT or BCAT. In this section, trap-detrap site inside drain region will be distinguished from the other trap-detrap site type (inside dielectric or at interface) and the depth equation of this trap-detrap site will be derived.

Table 4.1 indicates the time constants (τ_c and τ_e) variation with V_{DG} and V_B . Unlike the trap-detrap site inside dielectric or at interface, the trap-detrap site inside drain region have the time constants dependence on V_B , whereas the trap-detrap site inside dielectric or at interface have no time constants dependence on V_B .

Fig. 4.2 demonstrates the V_B dependence of time constants using the energy band diagram at the drain-to-body junction (AA') assuming that the trap-detrap site is located inside depletion region of drain. The energy band diagram in body region is shifted upward as more negative bias is applied in body (red line). This results in the increase of $E_T - E_{fn}$, which suggests that the probability for hole-capturing into the trap-detrap site

increases (τ_c decrease and τ_e increase). On the other hand, if the trap-detrap site is located in the neutral region of drain, τ_c and τ_e has weak dependance on V_B .

TABLE 4.1. The time constant variation with V_{DG} and V_B in case of trap-detrap site inside drain region.

Time constants variation with V_{DG}	$\tau_c \uparrow$ $\tau_e \downarrow$
Time constants variation with V_B	O

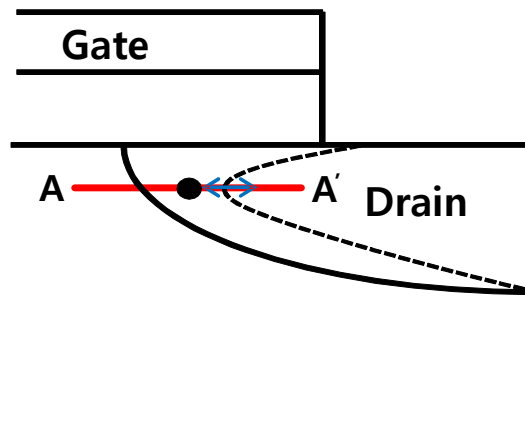


Fig. 4.1. The trap-detrap site inside drain region causing RTN in GIDL current.

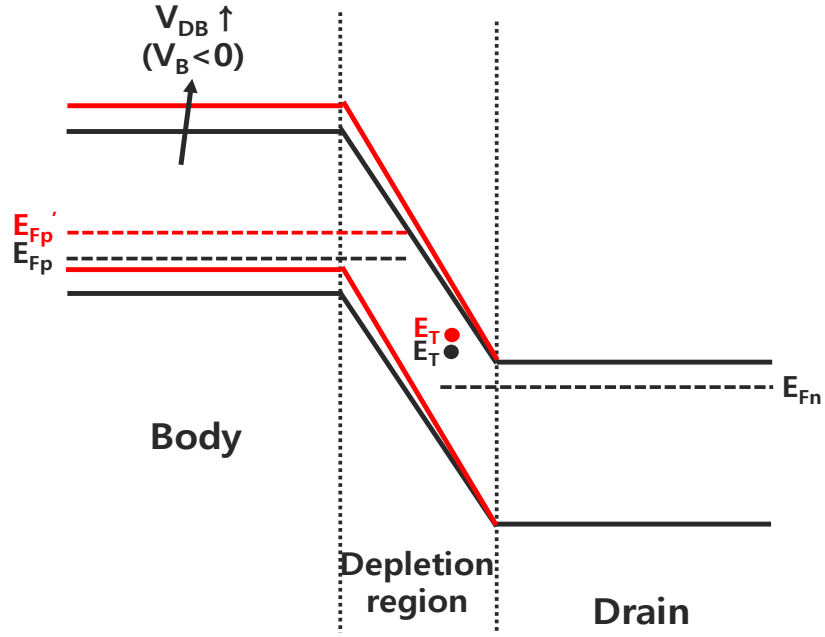


Fig. 4.2. The energy band diagram variation in drain-to-body junction as more negative V_B is applied. (AA' in Fig. 4.1)

The derivation procedures for the depth of trap-detrapped site inside drain region (x_{TSi}) will be explained briefly. The fundamental equation for depth extraction of trap-detrapped site is as follows [25]:

$$\ln\left(\frac{\tau_c}{\tau_e}\right) = \frac{1}{kT}(E_T - E_F) \quad (4.1)$$

where E_T is the energy level of trap-detrapped site, and E_F is the Fermi level.

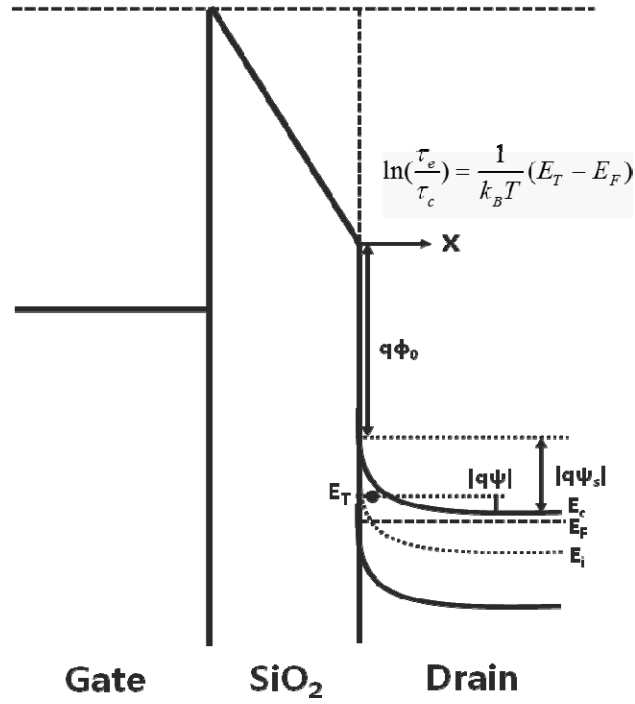


Fig. 4.3. The energy band diagram and related parameters for deriving the depth of trap-detrap site located inside silicon region.

$$E_T = q\phi_0 + (E_{cT} - E_T) + |\psi_s - \psi| \quad (4.2)$$

$$E_F = q\phi_0 + |\psi_s| + (E_{cD} - E_F) \quad (4.3)$$

In order to calculate surface potential at x_{TSi} (ψ), it is assumed that the shape of energy band in drain region in Fig. 4.3 is parabolic. Based on the above fact, ψ can be calculated using following simple equation [35]. In this equation, ψ_s is the surface potential at the drain neutral region which is represented in Ref. [11].

$$\psi = \psi_s \left(1 - \frac{x_T}{W_d}\right)^2 \quad (4.4)$$

where W_d is the width of depletion region in silicon, which is equal to $\sqrt{2\epsilon_{si} |\psi_s| / qN_D}$.

In the equation for W_d , ϵ_{si} the permittivity of silicon and N_D is the doping concentration of drain region. Using the equations from Eq. (4.1) to Eq. (4.4) and differentiating with V_{DG} , following equation can be represented as follows:

$$\frac{kT}{q} \frac{d \ln(\tau_e / \tau_c)}{dV_{DG}} = \frac{d|\psi_s|}{dV_{DG}} - x_{TSi} \sqrt{\frac{2qN_D}{\epsilon_{si}}} \frac{d\sqrt{|\psi_s|}}{dV_{DG}} \quad (4.5)$$

Where T is absolute temperature and k is the Boltzmann constant. Finally, arranging the Eq. (4.5) in terms of x_{TSi} , the final equation for the depth of trap-detrap site (x_{TSi}) extracting can be expressed.

$$x_{TSi} = \frac{\frac{d\psi_s}{dV_{DG}} + \frac{kT}{q} \frac{d \ln(\tau_e / \tau_c)}{dV_{DG}}}{\sqrt{\frac{qN_D}{2\epsilon_{si} |\psi_s|}} \frac{d\psi_s}{dV_{DG}}} = \sqrt{\frac{2\epsilon_{si} |\psi_s|}{qN_D}} \left[1 + \left(\frac{kT}{q} \frac{d \ln(\tau_e / \tau_c)}{dV_{DG}} \right) \frac{1}{\frac{d\psi_s}{dV_{DG}}} \right] \quad (4.6)$$

where T is absolute temperature and k is the Boltzmann constant. ϵ_{si} the permittivity of silicon, N_D is the doping concentration of drain region and ψ_s is the surface potential of

drain region.

4.3 TAT GIDL current RTN measurement in BCAT cell array

Fig. 4.4 shows the I_{GIDL} - V_D curves per 1 transistor with various temperatures in BCAT array. From this figure, the V_D range where TAT or BTB GIDL current mainly flow can be determined at each temperature. The region where I_{GIDL} has weaker dependence on V_D corresponds to the TAT GIDL current region.

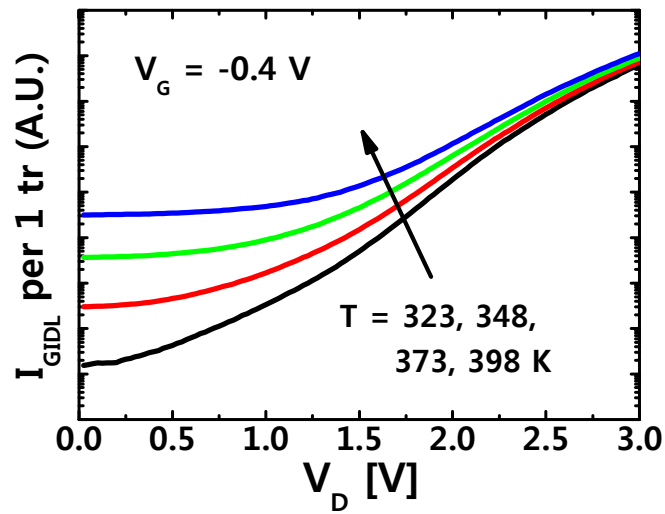


Fig. 4.4. Measured I_{GIDL} - V_D curves per 1 transistor with various temperatures in BCAT array ($V_G = -0.4 \text{ V}$)

And, the time-domain GIDL-current RTN as a function of V_B at 338 K are shown in Fig. 4.5 (a). In these measurements, gate voltage (V_G) was fixed to the -0.4 V. Considering the RTN-measured V_D range and Fig. 4.5 (a), it can be verified that GIDL RTN occurs at TAT current region in this sample. From the RTN measurement in the TAT GIDL current, capture time τ_c , and emission time τ_e as a function of V_B were extracted as shown in Fig. 4.5 (b). τ_c decreases with V_B , whereas τ_e increases with V_B . Based on the V_B dependence of time constants, it can be determined that the trap-detrap site causing GIDL RTN in TAT current region is located inside silicon (drain region).

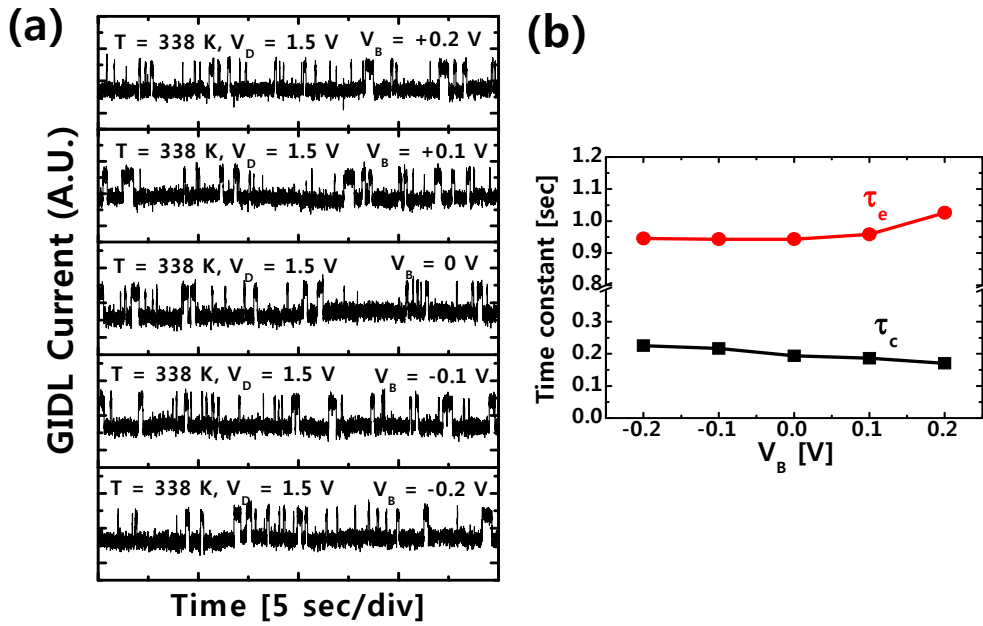


Fig. 4.5. (a) Measured time-domain GIDL RTN in TAT current with an increase in V_B at 338 K, (b) extracted capture time (τ_c) and emission time (τ_e) with an increase V_D .

The time-domain GIDL-current RTN as a function of V_D at 338 K are also shown in Fig. 4.6 (a). In Fig. 4.6, hole trapping into the trap-detrap site is considered instead of electron trapping. From this RTN measurement, τ_c , τ_e , and time constant ratio $\ln(\tau_e/\tau_c)$ as a function of V_D were extracted as shown in Fig. 4.6 (b) and (c). τ_c decreases with V_D , whereas τ_e increases with V_D . Using the linear slope of $\ln(\tau_e/\tau_c)$ with V_D and equations in Eq. 4.6, we can extract the depth (x_{TSi}) and energy level ($E_{CT} - E_T$) of trap-detrap site. The extracted value of x_{TSi} and $E_{CT} - E_T$ are 2.02 nm and 0.26 eV, respectively. Fig. 4.7 indicates x_T and $E_{CT} - E_T$ of this trap-detrap site in an energy band diagram.

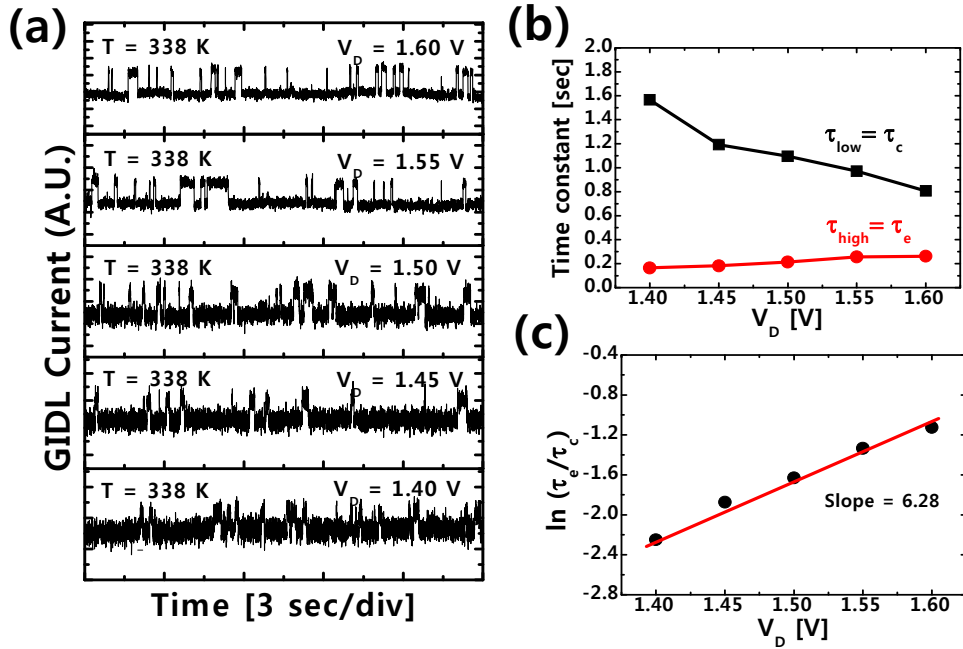


Fig. 4.6. (a) Measured time-domain GIDL RTN in TAT current with an increase in V_D at 338 K, (b) extracted capture time (τ_c) and emission time (τ_e) with an increase V_D , and (c) the ratio of τ_e to τ_c [$\ln(\tau_e / \tau_c)$] and its linear slope with an increase in V_D .

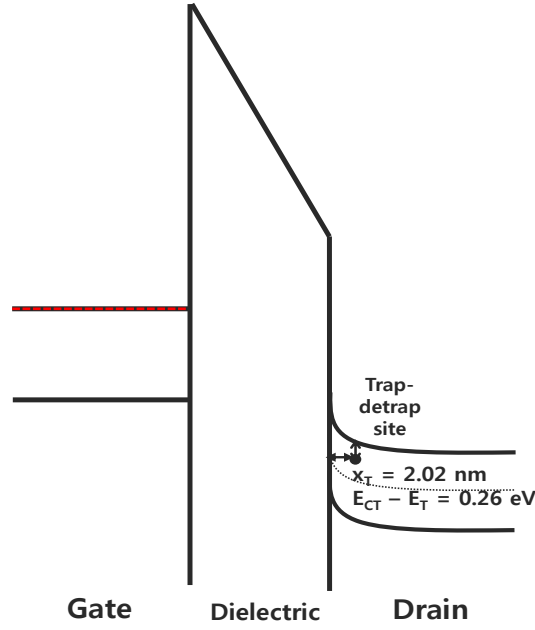


Fig. 4.7. The depth (x_{TSI}) and energy level ($E_{Cox} - E_T$) of measured trap-detrapping site.

On the other hand, the time-domain GIDL-current RTN as a function of V_B at 348 K are shown in Fig. 4.8 (a). From the RTN measurement in the TAT GIDL current, τ_c and τ_e as a function of V_B were extracted as shown in Fig. 4.8 (b). Because there are no V_B dependence of time constants, it can be determined that the trap-detrapping site causing GIDL RTN in TAT current region is not trap-detrapping site located inside drain region but trap-detrapping site inside dielectric.

In order to extract the depth and energy level of this trap-detrapping site, the time-domain GIDL-current RTN as a function of V_D at 348 K are measured as shown in Fig. 4.9 (a). From this RTN measurement, τ_c , τ_e , and time constant ratio $\ln(\tau_c/\tau_e)$ as a function of V_D were extracted as shown in Fig. 4.9 (b) and (c). τ_c increases with V_D , whereas τ_e decreases

with V_D . Using the linear slope of $\ln(\tau_c/\tau_e)$ with increase in V_D and equations mentioned in chapter 1, x_{TDrain} and $E_{Cox}-E_T$ can be extracted as 0.37 nm and 4.02 eV, respectively.

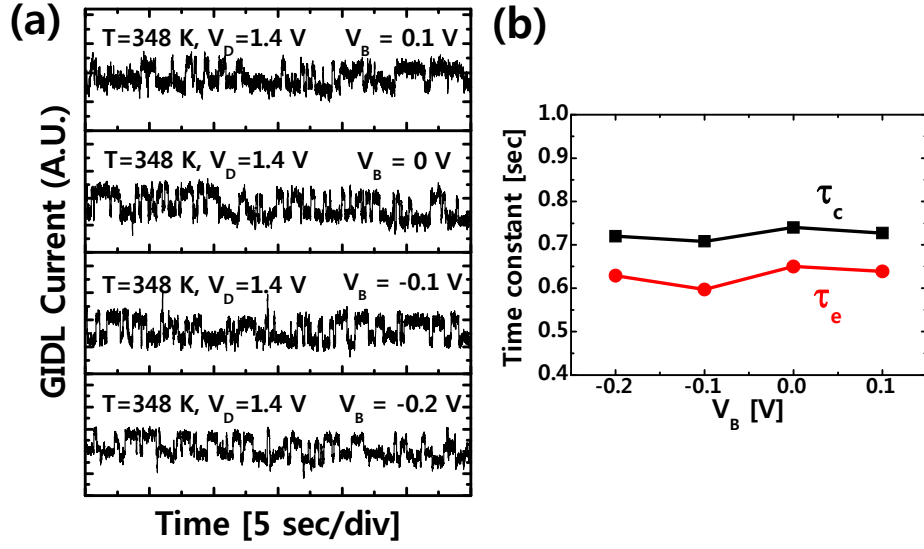


Fig. 4.8. (a) Measured time-domain GIDL RTN in TAT current with an increase in V_B at 338 K, (b) extracted capture time (τ_c) and emission time (τ_e) with an increase V_D .

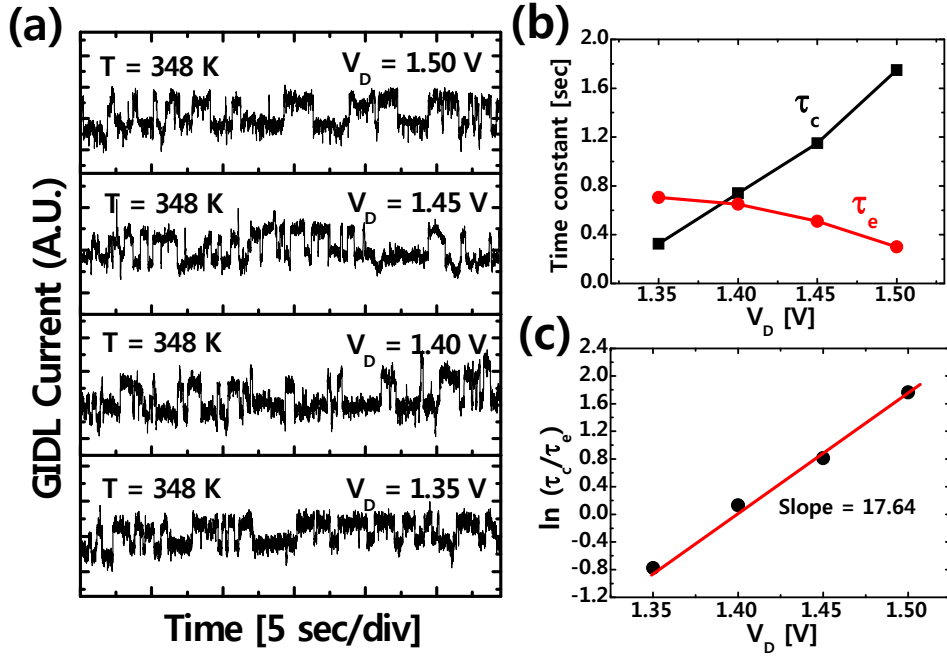


Fig. 4.9. (a) Measured time-domain GIDL RTN in TAT current with an increase in V_D at 338 K, (b) extracted capture time (τ_c) and emission time (τ_e) with an increase V_D , and (c) the ratio of τ_e to τ_c [$\ln(\tau_e / \tau_c)$] and its linear slope with an increase in V_D .

Fig. 4.10 (a) shows the measured I_{high}/I_{low} per 1 transistor with increase in V_D from the Fig. 4.6 (a). Fig. 4.10 (b) shows the plots for Eq. (5.4) & Eq. (5.5) and for the I_{high}/I_{low} value obtained in Fig. 4.10 (a) when $V_D = 1.5 \text{ V}$, $T = 338 \text{ K}$, and $x_T = 2.02 \text{ nm}$. The point of intersection between the two curves corresponds to the distance between the two trap sites. From the Fig. 4.10 (b), it can be noted that different r values are extracted with respect to the V_D . The equation for I_{filled}/I_{empty} can be represented as follows:

$$\frac{I_{filled}}{I_{empty}} = \exp\left(+\frac{q^2}{4\pi\epsilon_{eff}rkT}\right)(1 + g(F_{empty}))^{-1} \times \frac{F_{filled}}{F_{empty}} \exp\left[\frac{1}{F_{\Gamma}^2}(F_{filled}^2 - F_{empty}^2)\right] \quad (5.6)$$

In this equation, $g(F_{empty})$ term can be expressed using below equation [31].

$$g(F_{empty}) = \sqrt{\pi} \bar{E} \exp\left[\frac{\bar{E}^2}{3}\right] [2 - \operatorname{erfc}\left(-\frac{\bar{E}}{2}\right)] \quad (5.7)$$

In this equation, \bar{E} is equal to E/E_0 . And, E_0 can be represented to $8m_0m_t(kT)^3/q\hbar$. The equation for $\operatorname{erfc}(x)$ is the error complementary function. Fig. 4.11 (a) plots the r value with respect to V_D . The extracted r values are almost constant for different V_D value, which confirms the validity of the extraction result. The extracted r value is 2.13 nm. Fig. 4.11 (b) shows the cross-section of the positions of the two trap sites in the gate-to-drain overlap region of BCAT device. The x_T and r values extracted from Fig. 4.7 and 4.11 (a) can be used to accurately determine the relative positions of the trap sites causing RTN in the TAT GIDL current.

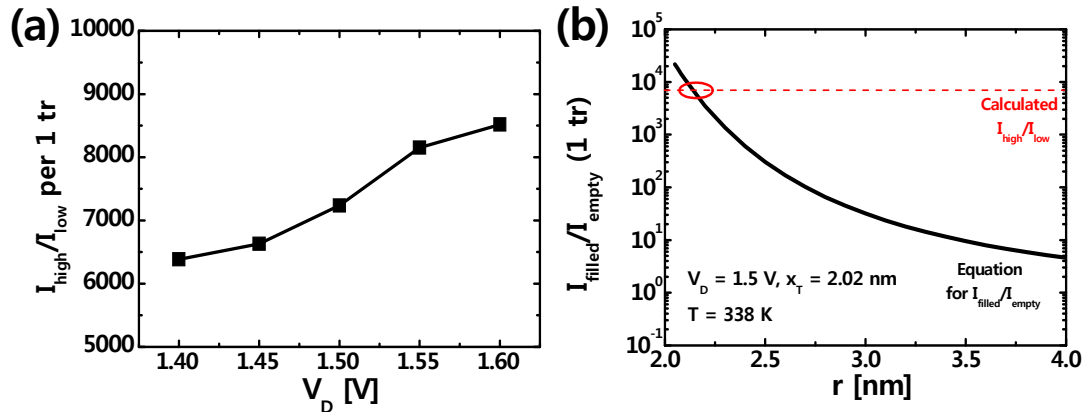


Fig. 4.10. (a) The calculated I_{high}/I_{low} per 1 transistor with increase in V_D and (b) the plot of calculated I_{high}/I_{low} per 1 transistor and equations for I_{filled}/I_{empty} .

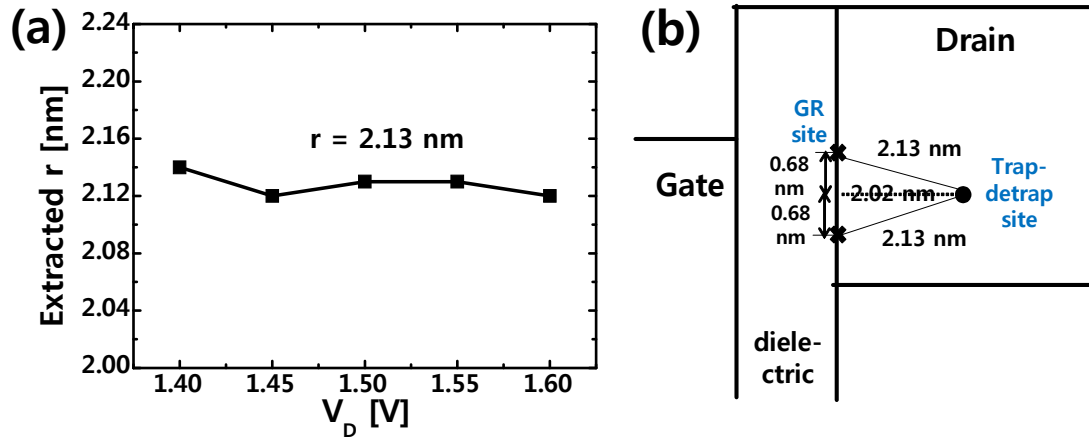


Fig. 4.11. (a) Extracted r with increase in V_D and (b) Illustration on the relative positions of two trap sites.

4.4 Summary

In this chapter, trap-detrap site inside drain region causing RTN in trap-assisted tunneling gate-induced drain leakage current was distinguished and actually measured in Buried cell array transistor for the first time. Finally, using the equations and methodologies mentioned in above chapters, the parameters related with the characteristics of trap-detrap and G-R site were extracted and analyzed.

5. Conclusion

In this thesis, the characteristics and trapping mechanism of trap sites in case of trap-detrap site inside dielectric or drain region causing RTN in TAT GIDL current were measured and analyzed based on the proposed equations and methodologies.

Based on the GIDL RTN measurement data in n-MOSFET, the distance between the two trap sites causing RTN in TAT GIDL current was accurately extracted for the oxide trap-detrap site by making proper use of the effective permittivity of two different materials.

The trapping mechanism was determined based on the activation energy comparison of capture and emission time. The electron trapping from conduction band was for the first time measured based on the smaller activation energy value of capture time as well as the electron trapping from valence band.

RTN in TAT GIDL current caused by trap-detrap site inside drain region was actually measured and analyzed in BCAT array. The parameters related with the characteristics of trap-detrap and G-R site were extracted and analyzed using the equations and methodologies explained in this thesis.

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초 록

DRAM cell에서 발생하는 variable retention time (VRT) 현상은 DRAM cell retention time을 열화시키는 주된 요인 중 하나이며, 최근 큰 문제가 되고 있다. 많은 연구를 통하여 VRT 현상은 GIDL 전류 영역 random telegraph noise (RTN)에 의해 발생한다는 것이 밝혀졌다. 그러므로, VRT 현상을 정확히 이해하기 위해서는 GIDL 전류 RTN의 원인이 되는 트랩에 대한 물리적 특성 이해가 반드시 이루어져야 한다. 현재까지는 band-to-band 터널링 영역에서의 GIDL 전류 RTN 연구가 주를 이루었고 이 전류 영역에서 RTN을 발생시키는 트랩 특성을 측정 데이터를 활용하여 추출하고 분석하는 연구가 많은 문헌들에서 이루어졌다. 하지만, 소자 축소화와 함께 동작 전압도 감소하면서 GIDL 전류가 주로 trap-assisted 터널링 (TAT)에 의하여 흐르기 때문에 이 전류 영역에서의 RTN 연구가 중요해진 상황이다. 다른 RTN 들과는 다르게 TAT 영역에서의 RTN은 2개의 트랩에 의하여 발생하기 때문에 더 많은 트랩 특성이 분석되어야 하지만 아직 TAT GIDL 전류에서의 RTN 연구는 부족하고 제한적인 범위에서만 연구가 진행된 상황이고 정확한 특성 추출을 하기에는 부족한 점들이 많다.

본 학위논문에서는 TAT GIDL 전류 RTN의 원인이 되는 두 트랩 (trap-detrapping site, generation-recombination site)들의 물리적 특성을 분석하는 연구를 진행하였다. 특히, MOSFET에서 trap-detrapping site가 절연체 내부에

존재할 때 TAT GIDL 전류 RTN을 실제 측정하여 각 트랩의 깊이나 에너지 레벨을 추출하였다. 또한, TAT GIDL 전류 RTN에서의 전류크기 비율과 두 물질의 유효 유전률을 활용하여 두 트랩 사이 거리를 정확히 추출하는 방법을 제안하고 실제로 추출하였다.

두번째, 전자가 trap-detrap site로 트랩핑될 때 어떤 메커니즘을 통해 트랩핑되는지 time constant들의 activation energy 대소 비교를 통하여 실제 측정 후 규명하였다.

마지막으로, MOSFET 뿐만 아니라 실제 DRAM cell로 사용되는 Buried-Gate CAT (BCAT)에서 TAT GIDL 전류영역 RTN을 실제로 측정하였다. 특히, 기존의 산화막 또는 계면에 존재했던 트랩뿐만 아니라 trap-detrap site가 실리콘 내부에 존재할 때 트랩의 물리적 성질을 추출하는 방법들을 제안하고 실제 이 경우에서 여러 가지 트랩 성질을 분석하였다. 본 학위논문에서 진행한 연구는 TAT GIDL 전류 영역에서의 RTN 현상을 이해하고 분석하는데 도움을 줄 수 있으며, 나아가서 VRT 현상을 이해하고 이를 줄일 수 있는 방법을 연구하는데 활용될 수 있을 것이다.

주요어 : Trap-assisted 터널링, GIDL 전류 RTN, trap-detrap site, 두 트랩 사이 거리, 트랩핑 메커니즘

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